

SIEMENS



Edition 1980/81

Design Examples of Semiconductor Circuits

SIEMENS

**Design Examples of
Semiconductor Circuits**

(Including also Applications with Software)

Edition 1980/81

(Follows directly after Edition 1978/79)

SIEMENS AKTIENGESELLSCHAFT

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1. RF Circuits

1.1 FM Tuner with MOS-Prestage

A FM tuner with MOS-prestage has been designed for top-quality radio models. The circuit is shown in **fig. 1.1**. The double-tuned input filter offers a good preselection. Extreme large signal characteristics are obtained by the MOS-prestage and the following symmetrical mixer-IC. A good signal-to-image ratio is realized by a double-tuned band-pass filter connected between prestage and mixer. The RF-signal is symmetrically supplied to IC S 042 P via a coupling coil. The oscillator voltage is also symmetrically coupled to the circuit via L_8 . Because of the symmetrical coupling an extremely high separation of RF- and oscillator-signal is achieved. On the one hand the oscillator is not pulled by high input voltages of the RF-signal, on the other hand the oscillator interference voltage at the secondary circuit of the band-pass filter is strongly suppressed because of the symmetrical coupling.

The oscillator signal is supplied via capacitor C_{12} to a buffer amplifier with BF 502 and then applied to a frequency divider with a ratio of 8:1. Frequency synthesis systems or frequency counters can be driven by this divider as already described.

The voltage generation for controlling the prestage operates as follows. A voltage is supplied from the secondary circuit of the first IF-filter, then applied via capacitor C_{28} to two diodes D_7 and D_8 and rectified. The control voltage is amplified by BC 238. This transistor converts the voltage to the right polarity being necessary for controlling gate 2 of the prestage transistor. That means terminal V_F has to be connected to $V_{contr.}$. By this controlling interference influences are reduced and the indication range of field strength is extended to 120 dB.

The IF output has a low impedance because of the common-emitter circuit. Therefore interference effects to the IF connection between tuner and IF amplifier are reduced.

Technical data

Supply voltages

$$V_{s1} = 15 \text{ V}$$

$$V_{s2} = 5 \text{ V}$$

Supply currents

$$I_{s1} = 33 \text{ mA}$$

$$I_{s2} = 120 \text{ mA}$$

Tuning voltage

$$V_D = 4.8 \text{ to } 28 \text{ V}$$

Power gain

$$G_p > 35 \text{ dB}$$

Noise figure

$$N < 5 \text{ dB}$$

RF bandwidth

$$B_{RF} < 1.2 \text{ MHz}$$

IF bandwidth

$$B_{IF} = 400 \text{ kHz}$$

Dynamic range

$$\Delta G_p > 50 \text{ dB}$$

Frequency drift of oscillator
because of temperature

$$\Delta f_0 < 2 \text{ kHz/K}$$

Coil data

L_1 1 turn

0.5 mm $\varnothing$ ECu

L_2 5 turns

0.8 mm $\varnothing$ CuAg

L_3 5 turns

0.8 mm $\varnothing$ CuAg tap at 3rd turn

L_4 6 turns

0.8 mm $\varnothing$ CuAg

L_5 5 turns

0.8 mm $\varnothing$ CuAg

L_6 2 turns

0.5 mm $\varnothing$ ECu

L_7 7 turns

0.5 mm $\varnothing$ ECu

L_8 2 turns

0.5 mm $\varnothing$ ECu

L_9 12 turns

0.2 mm $\varnothing$ ECu

L_{10} 2 turns

0.2 mm $\varnothing$ ECu

L_{11} 12 turns

0.2 mm $\varnothing$ ECu

$L_{1, 2, 3, 4, 5, 6, 7, 8}$

on coil former 4.3 mm $\varnothing$

$L_{1, 2, 3, 4, 5, 6}$

screw core B 63310-B 3021-X017

$L_{7, 8}$

screw core 3.5 $\times$ 0.5 5 $\times$ 10 (brass)

$L_{9, 10, 11}$

on Vogt coil former set D 41-2520

Ch

choke 6.8 μ H

Ferrite bead

B 62110 N22

Components for circuit 1.1

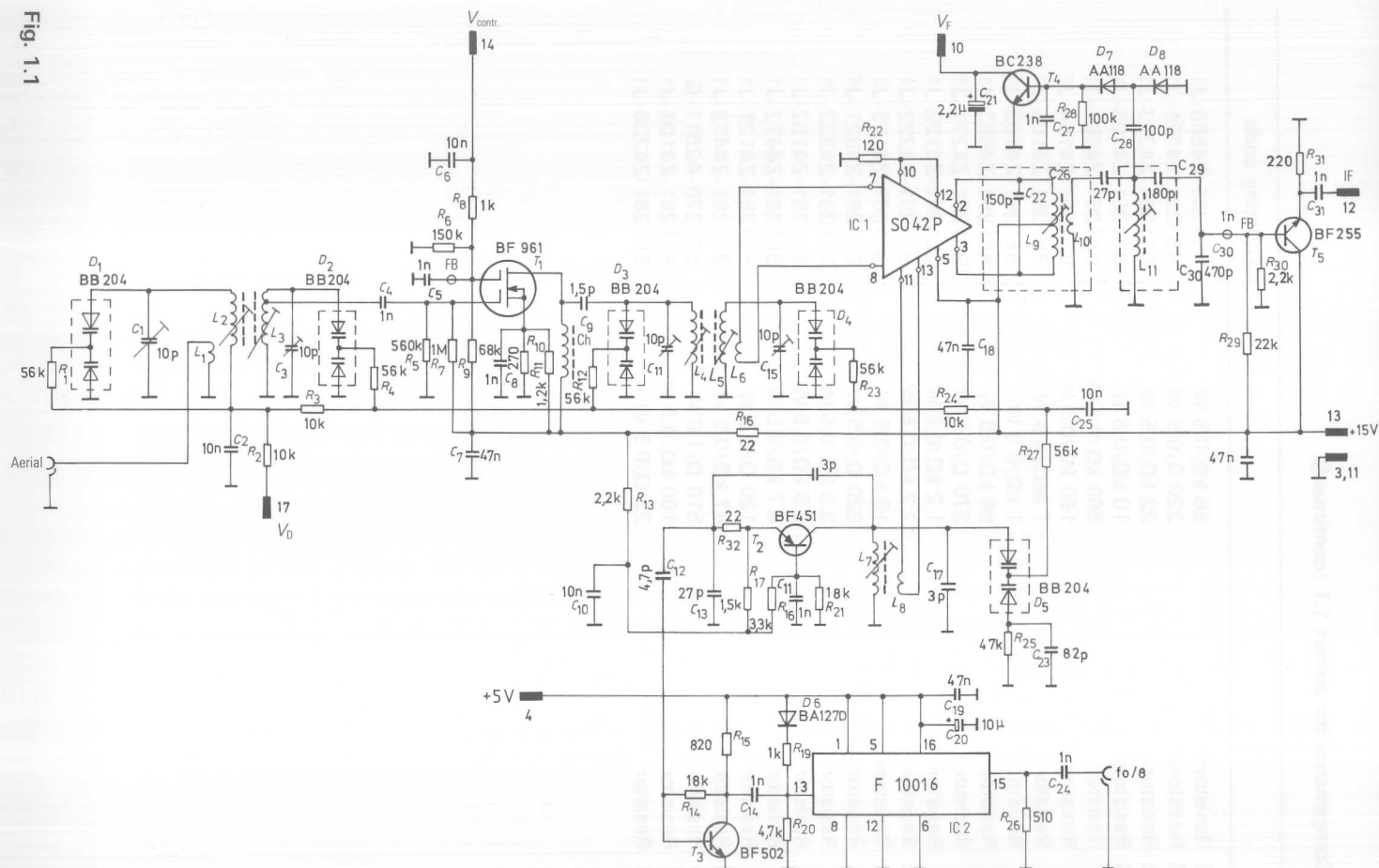
		Ordering code
1 MOS-transistor	BF 961	Q62702-F518
1 Transistor	BF 451	Q62702-F313
1 Transistor	BF 502	Q62702-F572
1 Transistor	BF 255	Q62702-F329
1 Transistor	BC 238	Q62702-F698
1 IC	S042P	Q67000-A335
1 Frequency divider 8:1	(F 10016)	—
5 Capacitance diodes	BB 204 green	Q62702-B57-X5
1 Diode	BA 127 d	Q60201-X127-D9
2 Diodes	AA 118	Q60101-X118
1 Ceramic capacitor	1.5 pF/63 V	B38060-A6010-C506
1 Ceramic capacitor	3.3 pF/63 V	B38062-A6030-C306
1 Ceramic capacitor	4.7 pF/63 V	B38062-A6040-C706
1 Ceramic capacitor	27 pF/63 V	B38062-A6270-G006
1 Styroflex capacitor	27 pF/160 V	B31063-B1270-H
1 Ceramic capacitor	82 pF/63 V	B38062-A6820-G006
1 Ceramic capacitor	100 pF/63 V	B38062-A6101-G006
1 Styroflex capacitor	150 pF/160 V	B31063-B1151-H
1 Styroflex capacitor	180 pF/160 V	B31063-B1181-H
1 Ceramic capacitor	470 pF/63 V	B32076-A6471-G006
8 Ceramic capacitors	1000 pF/250 V	B37462-B2102-S1
4 MKT capacitors	10 nF/63 V	B32509-A0103-M
1 Ceramic capacitor	47 nF/63 V	B37449-F6473-S2
2 MKT capacitors	47 nF/63 V	B32509-A0473-M
1 Electrolytic capacitor	2.2 μ F/63 V	B41313-A8225-T
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Screw core		B63310-B3021 X017
1 Ferrite bead		B62110

Components for circuit 1.1 (continued)

			Ordering code
5 Resistors	56 k Ω /0.5 W		B51261-Z4563-J1
2 Resistors	220 Ω /0.5 W		B50261-Z4221-J1
2 Resistors	22 k Ω /0.5 W		B51261-Z4223-J1
3 Resistors	10 k Ω /0.5 W		B51261-Z4103-J1
1 Resistor	560 k Ω /0.5 W		B51261-Z4564-J1
1 Resistor	150 k Ω /0.5 W		B51261-Z4154-J1
1 Resistor	1 M Ω /0.5 W		B51261-Z4105-J1
1 Resistor	1 k Ω /0.5 W		B51261-Z4102-J1
1 Resistor	68 k Ω /0.5 W		B51261-Z4683-J1
1 Resistor	270 Ω /0.5 W		B51261-Z4271-J1
1 Resistor	1.2 k Ω /0.5 W		B51261-Z4122-J1
2 Resistors	2.2 k Ω /0.5 W		B51261-Z4222-J1
2 Resistors	18 k Ω /0.5 W		B51261-Z4183-J1
1 Resistor	820 Ω /0.5 W		B51261-Z4821-J1
1 Resistor	3.3 k Ω /0.5 W		B51261-Z4332-J1
1 Resistor	1.5 k Ω /0.5 W		B51261-Z4152-J1
1 Resistor	4.7 k Ω /0.5 W		B51261-Z4472-J1
1 Resistor	120 Ω /0.5 W		B51261-Z4121-J1
1 Resistor	47 k Ω /0.5 W		B51261-Z4473-J1
1 Resistor	510 Ω /1.0 W		B51276-A2511-G
1 Resistor	100 k Ω /0.5 W		B51261-Z4104-J1
1 Resistor	22 Ω /0.5 W		B51261-Z4220-J1

Fig. 1.1

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1.2 FM IF-Amplifier with High Selectivity

The circuit shown in **fig. 1.2** offers an extremely high adjacent-channel selectivity, being realized by two ceramic filters. Both are coupled by transistor T_4 . Because of the inverse feedback achieved by resistors R_{10} and R_{21} the two transistors T_2 and T_4 operate linearly in the total dynamic range of the tuner.

The IC TDA 1047 with integrated coincidence demodulator operates as main IF-amplifier. A low distortion factor is realized by using a band-pass filter as demodulator circuit. The noise suppression depends on field strength and mistuning. Its threshold can be adjusted by potentiometer P_7 and the muting depth is set by potentiometer P_5 . The stereo-threshold is adjusted by potentiometer P_6 . An AF amplifier with transistor T_6 is additionally connected to the demodulator circuit.

A special feature is realized by IC₂, a quadruple operational amplifier. It considers the field strength information from the FM tuner, from the FM-IF-circuit and the AM-circuit. Therefore a continuous indication is attained at a small as well as a great field strength. The device automatically changes from FM to AM range.

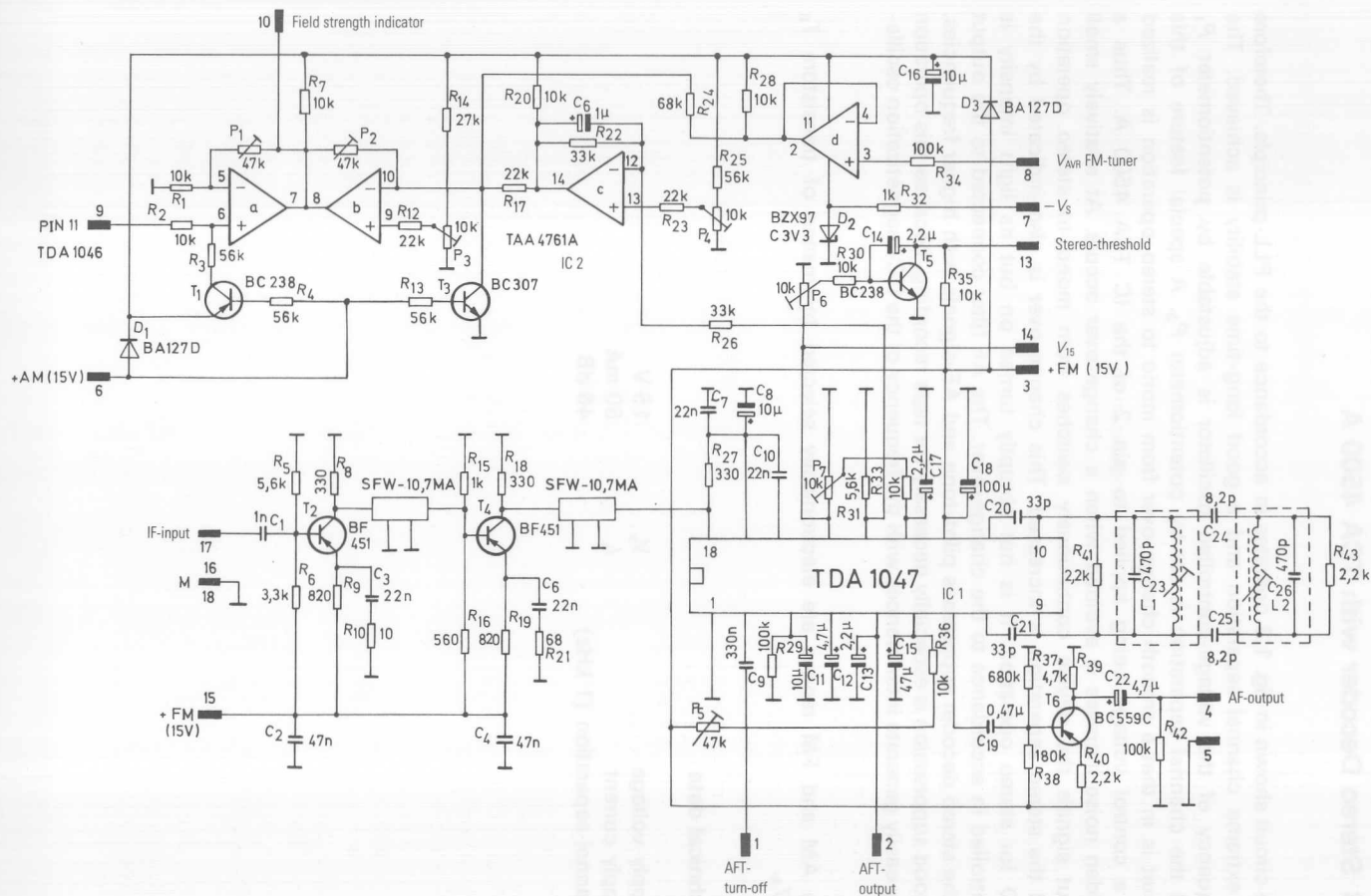
Technical data

Supply voltage	15 V
Supply current	45 mA
Sensitivity at a signal-to-noise ratio of 26 dB	12 dB/ μ V
Limiting range	23 dB/ μ V
Signal-to-noise ratio	> 70 dB
AM suppression	> 65 dB
Adjacent-channel rejection	> 80 dB
Distortion factor ($d=75$ kHz)	0.25%
AF output voltage	0.5 V
Range on field strength indication	120 dB

Components for circuit 1.2

		Ordering code
1 FM IF-amplifier with demodulator	TDA 1047	Q67000-A1091
1 Quad opamp	TAA 4761 A	Q67000-A1032
2 Transistors	BC 238	Q62702-C698
1 Transistor	BC 559 C	Q62702-C695-V3
2 Transistors	BF 451	Q62702-F313
1 Z-diode	BZX 97/C3V3	Q62702-Z1223-F82
2 Diodes	BA127D	Q60201-X127-D9
2 Ceramic capacitors	8.2 pF/63 V	B38062-A6080-C206
2 Ceramic capacitors	33 pF/63 V	B38062-J6330-G006
2 Styroflex capacitors	470 pF/160 V	B31063-B1471-H
1 Ceramic capacitor	1 nF/250 V	B37462-J2102-S1
4 Ceramic capacitors	22 nF/63 V	B37449-F6223-S2
2 MKT-capacitors	47 nF/63 V	B32509-C473-M
1 MKT-capacitor	330 nF/100 V	B32510-D1334-K
1 MKT-capacitor	470 nF/100 V	B32510-D1374-K
1 Electrolytic capacitor	1 μ F/40 V	B41313-A7105-V
3 Electrolytic capacitors	2.2 μ F/63 V	B41313-A8225-T
2 Electrolytic capacitors	4.7 μ F/40 V	B41313-A7475-T
3 Electrolytic capacitors	10 μ F/25 V	B41313-A5106-T
1 Electrolytic capacitor	47 μ F/25 V	B41283-A5476-T
1 Electrolytic capacitor	100 μ F/25 V	B41283-A5107-T
1 Resistor	10 Ω /0.5 W	B51261-Z4100-J1
1 Resistor	68 Ω /0.5 W	B51261-Z4680-J1
3 Resistors	330 Ω /0.5 W	B51261-Z4331-J1
1 Resistor	560 Ω /0.5 W	B51261-Z4561-J1
2 Resistors	820 Ω /0.5 W	B51261-Z4821-J1
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
3 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
2 Resistors	5.6 k Ω /0.5 W	B51261-Z4562-J1
9 Resistors	10 k Ω /0.5 W	B51261-Z4103-J1
3 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
1 Resistor	27 k Ω /0.5 W	B51261-Z4273-J1
2 Resistors	33 k Ω /0.5 W	B51261-Z4333-J1
4 Resistors	56 k Ω /0.5 W	B51261-Z4563-J1
1 Resistor	68 k Ω /0.5 W	B51261-Z4683-J1
3 Resistors	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	180 k Ω /0.5 W	B51261-Z4184-J1
1 Resistor	680 k Ω /0.5 W	B51261-Z4684-J1

Fig. 1.2



1.3 Stereo Decoder with TCA 4500 A

The circuit shown in **fig. 1.3** operates in accordance to the PLL-principle. Therefore an extreme channel separation and a good long-time stability is achieved. The frequency of the voltage-controlled oscillator is adjustable by potentiometer P_1 and the channel separation is set by potentiometer P_2 . A special feature of this circuit is in that a smooth change-over from mono to stereo operation is realized by a control voltage being applied to pin 2 of the IC TCA 4500 A. Thus a sudden noise increase is avoided when a change-over occurs. At relatively small input signals the device continuously switches from mono to stereo operation and the stereo separation is increased. This change-over is also indicated by the LED for stereo operation. It is not abruptly turned on but its light intensity is controlled in accordance to the change-over. The AF filter connected to the output of the stereo decoder suppresses pilot-tone and AF-signals with higher frequencies. A good suppression is especially necessary for tape recording, because this operation may easily generate interferences with the frequency of the DC-magnetization oscillator.

The AM and FM ranges are electronically selected by means of transistors T_6 to T_9 .

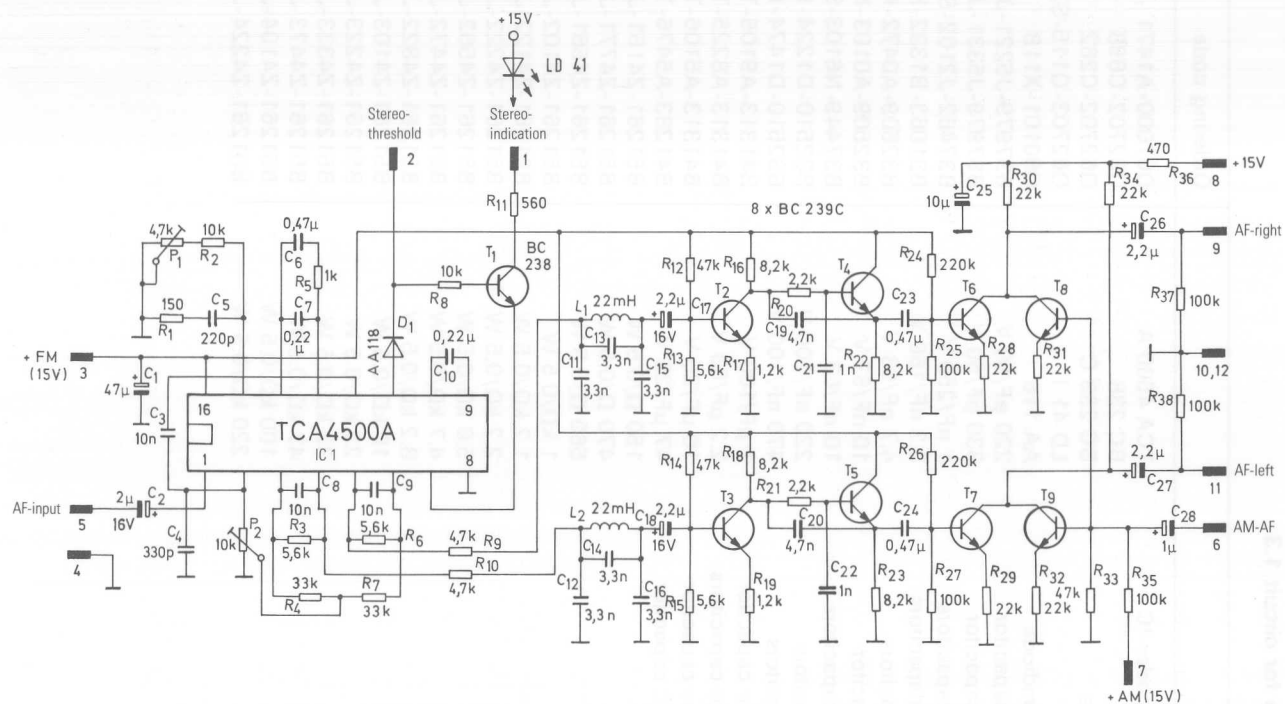
Technical data

Supply voltage	V_s	15 V
Supply current	I_s	60 mA
Channel separation (1 kHz)		46 dB

Components for circuit 1.3

		Ordering code
1 Stereo decoder-IC	TCA 4500 A	Q67000-A1471
1 Transistor	BC 238	Q62702-C698
8 Transistors	BC 239 C	Q62702-C282
1 LED	LD 41 I	Q62703-Q115-S2
1 Germaniumdiode	AA 118	Q60101-X118
1 Ceramic capacitor	220 pF/50 V	B37979-J5221-J
1 Ceramic capacitor	330 pF/50 V	B37979-J5331-J
2 Ceramic capacitors	1 nF/250 V	B37462-J2102-S1
6 Styroflex capacitors	3.3 nF/160 V	B31063-B1332-H
2 MKT capacitors	4.7 nF/63 V	B32509-A0472-M
1 MKT capacitor	10 nF/63 V	B32509-A0103-M
2 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
2 MKT capacitors	220 nF/100 V	B32510-D1224-K
3 MKT capacitors	470 nF/100 V	B32510-D1474-K
1 Electrolytic capacitor	1 μ F/100 V	B41313-A9105-T
5 Electrolytic capacitors	2.2 μ F/63 V	B41313-A8225-T
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Electrolytic capacitor	47 μ F/25 V	B41283-A5476-T
1 Resistor	150 Ω /0.5 W	B51261-Z4151-J1
1 Resistor	470 Ω /0.5 W	B51261-Z4771-J1
1 Resistor	560 Ω /0.5 W	B51261-Z4561-J1
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
2 Resistors	1.2 k Ω /0.5 W	B51261-Z4122-J1
2 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
4 Resistors	5.6 k Ω /0.5 W	B51261-Z4562-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
4 Resistors	8.2 k Ω /0.5 W	B51261-Z4822-J1
2 Resistors	10 k Ω /0.5 W	B51261-Z4103-J1
6 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
2 Resistors	33 k Ω /0.5 W	B51261-Z4333-J1
3 Resistors	47 k Ω /0.5 W	B51261-Z4473-J1
5 Resistors	100 k Ω /0.5 W	B51261-Z4104-J1
2 Resistors	220 k Ω /0.5 W	B51261-Z4224-J1

Fig. 1.3



1.4 Broadband Chain-Amplifier with $8 \times \text{CFY 11}$

The GaAs-Shottky-barrier FET, type CFY 11, is suitable for applications of up to 14 GHz. It features an extremely low input noise figure. Due to its high gain and its good linearity this transistor is favoured for applications of telecommunication systems as well as of digital systems requiring small switching times. Input and output impedances are relatively constant in a range of up to 1 GHz. **Fig. 1.4** shows the circuit of a chain amplifier. The coils are realized by resonant-line circuits. Two of its L-sections are connected each between the drain terminals and between the gate terminals. The gate and drain reactances realize the shunt capacitance of the low-pass circuits. Inputs and outputs are terminated by an L-network each.

A schematic drawing of the circuit being realized on teflon substrate can be obtained from the Siemens sales organisation.

Technical data

Frequency range	1 MHz to 2.5 GHz
Input reflection factor	<0.2
Output reflection factor	<0.3
Gain	>14 dB
Backward gain	<0.04
Noise figure	<3.8 dB
Range of linear output voltage ($R_G = R_L = 50 \Omega$, $d_{IM} = 60$ dB, $f = 800$ MHz)	550 mV

Components for circuit 1.4

		Ordering code
8 GaAs-FETs	CFY 11 C11	Q62703-F0001
3 Ceramic chip-capacitors	47 nF/50 V	B37947-B5473-K9
2 RF chokes	100 μH	B78108-S1104-J

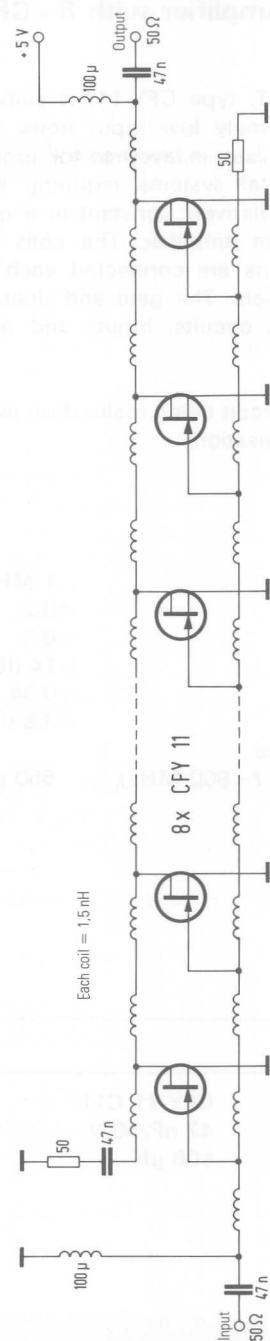


Fig. 1.4

1.5 Double-Superheterodyning Receiver for SW Range Using S 054 T

Only with a little elaborateness of components a top-quality AM receiver can be designed by using S 054 T and TDA 1046 as amplifying ICs. The circuit operates in accordance to the principle of double-heterodyning and therefore especially good features are realized in the SW range. In the MW range a MOS prestage with transistor BF 961 is additionally used.

Because of its low series impedance two diodes, type BB 709, are utilized for tuning in the SW range and one BB 312 in the MW range. The adequate frequency range is selected by 4 switching diodes, type BA 282, two BA 127 d and one AF-transistor BC 307 B.

SW stage

For a good reception of a station in the SW range the following features are extremely important: signal-to-image ratio, large signal characteristics and automatic gain control. A good signal-to-image ratio can be only obtained by double-heterodyning. Besides that the used IC, type S 054 T, offers the advantage in that only few components are required as shown in **fig. 1.5.1**.

The front end is matched to 50 Ω . Circuits of short rod-aerials can be directly connected to the aerial input but an outdoor aerial has to be inductively coupled to the front end. In this case the turns of the coupling coil have to be varied (see **fig. 1.5.2**).

The front end incorporates two coupling coils realized by a single-layer solenoid. The front end circuit as well as the oscillator are tuned by a capacitance diode each, type BB 709, which is especially favoured for applications in the SW range as it features a low series impedance and a high capacitance ratio. Thus tuned circuits with a relatively high Q can be realized in the SW-range.

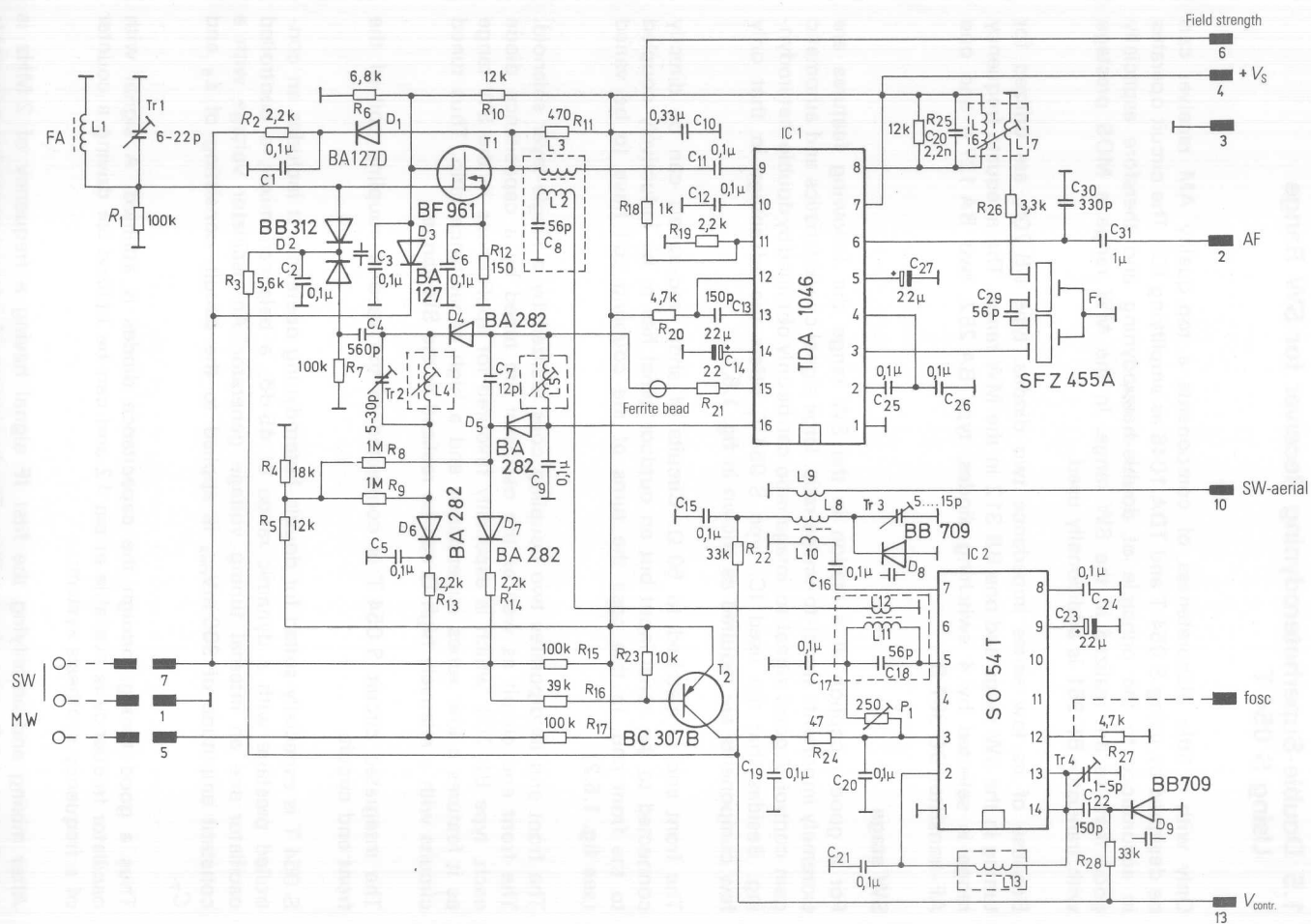
The integrated circuit S 054 T is connected to the second coupling coil of the front end circuit.

S 054 T is especially suited for double-heterodyning operation. It includes an controlled prestage with a dynamic range of 45 dB, a balanced mixer, a controlled oscillator and an internal tuning voltage generator. An oscillator voltage with a constant amplitude of 300 mV_{rms} is applied to the circuit, consisting of L_5 and C_7 .

Thus a good tuning through the capacitance diodes is attained. A signal with oscillator frequency is available at pin 12 and can be utilized for driving a counter of a frequency synthesis system.

After mixing and amplifying the first IF signal having a frequency of 2 MHz is supplied to the first band-pass filter. The beginning of internal control is adjustable by potentiometer P_1 . It is connected from pin 3 of the IC to coil L_{11} . For the

Fig. 1.5.1



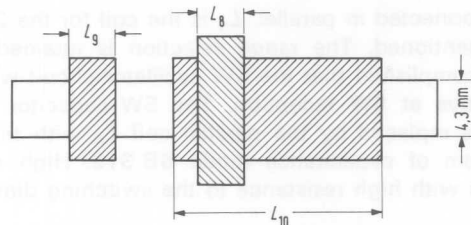


Fig. 1.5.2

described application example it is advantageous to adjust a late, i.e. a delayed beginning of the control to realize a good signal-to-noise ratio. The control starts at approx. 0.15 mV (EMF, $R_i = 50 \Omega$).

The 2 MHz-bandpass-filter for the first IF is capacitively coupled and offers a high Q. The signal is applied to the TDA 1046 via the coupling winding L_3 .

As for reception in the SW range the MW prestage with BF 961 has to be short-circuited, gate 2 being normally on a level of 4.5 V is now set to a level of 0.7 V by a diode. The drain is connected to ground via a capacitor and a diode being operated in forward direction. Therefore strong stations of the MW range cannot interfere.

TDA 1046 is a complete AM-receiver IC. An IF signal with a frequency of 2 MHz is supplied to this IC when a station of the SW range is received. The oscillator circuit oscillates with a frequency of 2.455 MHz. Thus an IF of 455 kHz is generated.

It has to be mentioned that a 22Ω -resistor with a ferrite bead is connected in series to the oscillator circuit of the TDA 1046. Thus parasitic oscillations are avoided. The ferrite bead has to be glued.

MW stage

A station of the MW range is received by the ferrite rod coil. The signal is amplified by the MOS-tetrode BF 961. This has the advantage in that a higher gain and a better signal-to-noise ratio are achieved and that a coupling coil for the IC is not necessary.

As the front end circuit is not essentially loaded by the BF 961 the bandwidth of the ferrite-rod aerial circuit can be optimized. The Q of the aerial coil can be lower and therefore the construction of the coil is simplified.

The front end circuit is tuned by one system of the capacitance diode BB 312. The RF signal is amplified by the MOS-tetrode and supplied from the drain to the input of TDA 1046 via a coupling winding of the 2 MHz-bandpass-filter which selects the first IF when a station in the SW range is received. Interferences by SW transmitters cannot occur as the S 054 T is turned off during MW reception.

The voltage of the oscillator circuit being tuned by a capacitance diode is also controlled. It has an internal feedback. The inductance of the circuit is realized

by coils L_4 and L_5 connected in parallel. L_5 is the coil for the 2.455 MHz-oscillator circuit as already mentioned. The range selection is attained by four switching diodes. Thus it is accomplished that the SW oscillator circuit with its fixed capacity becomes only effective at SW reception. The SW-capacitor C_7 is by-passed at MW reception and is replaced by the parallel coil L_4 with trimmer capacitor and by the second system of capacitance diode BB 312. High reverse voltages are supplied via resistors with high resistance to the switching diodes.

The IC TDA 1046 is responsible for mixing, amplifying and demodulation of the IF signal. The AF signal is available at pin 6.

Technical data

Supply voltage $V_s = 12\text{ V}$
 Supply current $I_s = 43\text{ mA}$ at SW
 Supply current $I_s = 24\text{ mA}$ at MW
 Range of SW reception from 5.8 to 11 MHz
 Range of MW reception from 520 to 1640 kHz
 Tuning voltage 1 to 28 V
 1st intermediate frequency (SW) = 2 MHz
 2nd intermediate frequency (MW) = 455 kHz

Signal-to-noise factor for SW-range:

Input voltages

Signal-to-noise factor	(EMF at 50 Ω); ($f=6.8$ and 10 MHz)
10 dB	3.2 to 4 μV
20 dB	9.5 to 12 μV
26 dB	20 to 26 μV
40 dB	100 to 160 μV

Signal-to-noise factor for MW range:

Signal-to-noise factor	Field strength
10 dB	0.072 to 0.1 mV/m
20 dB	0.27 to 0.32 mV/m
26 dB	0.52 to 0.9 mV/m
40 dB	2.7 to 3.3 mV/m

Bandwidth of front end circuit at SW reception

f_{in}	6 MHz	8 MHz	10 MHz
$B_{3\text{ dB}}$	120 kHz	160 kHz	290 kHz

1st intermediate frequency (2 MHz)

$$B_{3\text{dB}} = 30 \text{ kHz}$$

2nd intermediate frequency (455 kHz)

$$B_{3\text{dB}} = 4.5 \text{ kHz}$$

Signal-to-image selection at SW reception:

f_{in}	6 MHz	10 MHz
a_s	48 dB	35 dB

Bandwidth of ferrite-rod aerial circuit at MW reception:

f_{in}	0.6 MHz	1 MHz	1.6 MHz
$B_{3\text{dB}}$	7 kHz	13.5 kHz	31 kHz

Coil data

$L_1 = 45$ turns	12×0.05 ESSCu
$L_2 = 85$ turns	4×0.05 ESSCu
$L_3 = 8$ turns	4×0.05 ESSCu
$L_4 = 140$ turns	4×0.05 ESSCu
$L_5 = 110$ turns	4×0.05 ESSCu
$L_6 =$	IF-filter of General Instruments Colour code red-blue
$L_7 =$	
$L_8 = 60$ turns	3×0.05 ESSCu
$L_9 = 3$ turns	3×0.05 ESSCu
$L_{10} = 5$ turns	3×0.05 ESSCu
$L_{11} = 85$ turns	4×0.05 ESSCu
$L_{12} = 1$ turn	4×0.05 ESSCu
$L_{13} = 30$ turns	4×0.05 ESSCu

L_1 on ferrite rod, ordering code B61610-J1017-X025 (Siemens)

$L_{2, 3, 5, 11, 12, 13}$ on Vogt-filter set D41-2520

L_4 on Vogt-filter set D41-2640

$L_{8, 9, 10}$ on Vogt-coil former 313 20 000 00

Ferrite-screw core, ordering code B63310-B3021-X012 (Siemens)

Ferrite bead N22, ordering code B62110-A3011-X022 (Siemens)

Components for circuit 1.5

		Ordering code
1 IC	S 054 T	Q67000-A1472
1 IC	TDA 1046	Q67000-A1092
1 MOS-Transistor	BF 961	Q62702-F518
1 Transistor	BC 307 B	Q62702-C324
1 Double capacitance diode	BB 312	Q62702-B143
2 Capacitance diodes (paired)	BB 709	Q62702-B169
4 Switching diodes	BA 282	Q62702-A428
2 Diodes	BA 127 D	Q60201-X127-D9
1 Ceramic capacitor	12 pF/63 V	B38062-B6120-G6
3 Ceramic capacitors	56 pF/63 V	B38062-B6560-G6
2 Ceramic capacitors	150 pF/63 V	B38062-B6151-G6
1 Ceramic capacitor	330 pF/50 V	B38112-A5331-K
1 Ceramic capacitor	560 pF/63 V	B37062-A6561-K6
1 Styroflex capacitor	2200 pF/160 V	B31063-B1222-H
18 MKT-capacitors	100 nF/100 V	B32509-C1104-M
1 MKT-capacitor	330 nF/100 V	B32510-D1334-K
3 Ta-electrolytic capacitors	22 μ F/26 V	B41181-B2226-M
1 Screw core		B63310-B3021-X12
1 Ferrite bead		B62110-A3011-X22
1 Ferrite rod		B61610-J1017-X25
1 Resistor	22 Ω /0.5 W	B51261-Z4220-J1
1 Resistor	47 Ω /0.5 W	B51261-Z4470-J1
1 Resistor	150 Ω /0.5 W	B51261-Z4151-J1
1 Resistor	470 Ω /0.5 W	B51261-Z4471-J1
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
4 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	5.6 k Ω /0.5 W	B51261-Z4562-J1
1 Resistor	6.8 k Ω /0.5 W	B51261-Z4682-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
3 Resistors	12 k Ω /0.5 W	B51261-Z4123-J1
1 Resistor	18 k Ω /0.5 W	B51261-Z4183-J1
2 Resistors	33 k Ω /0.5 W	B51261-Z4333-J1
1 Resistor	39 k Ω /0.5 W	B51261-Z4393-J1
4 Resistors	100 k Ω /0.5 W	B51261-Z4104-J1
2 Resistors	1 M Ω /0.5 W	B51261-Z4105-J1
1 Ceramic filter	SFZ 455 A (Fa. Murata)	

1.6 Frequency Synthesizer for VHF Range Using MOS-IC S 187

Digital tuning is successfully applied for radio telecommunication devices (e.g. CB, police radio, taxi hire service) and for radio receivers as the required MOS-LSI-circuits become more and more economical. If more than 5 stations have to be tuned with crystal accuracy the frequency synthesis system is cheaper. By utilizing the IC S 187 and a crystal only, more than 500,000 different frequencies can be tuned if required. Each individual frequency has the same accuracy and constance as the one of the reference oscillator being crystal-controlled.

Function of PLL-frequency synthesis

Fig. 1.6.1 shows the block diagram of a frequency synthesizer with S 187 for the VHF range between 155.77 and 155.95 MHz. The channel spacing is 20 kHz. The PLL-circuit digitally compares the frequency to be controlled and a crystal-controlled reference frequency. In dependence on frequency and phase a control voltage is generated by an integration circuit (LP). This voltage controls the capacitance diode of a voltage controlled oscillator (VCO).

The crystal-controlled frequency of 3.2 MHz is processed in a divider with a ratio of 640 and applied to the input of the phase comparator. Thus a reference frequency of 5 kHz is generated. At input 2 of the phase comparator a signal with a frequency, derived from the one of the VCO, is applied. If this frequency is in the locking range the capacitance diode of the VCO is tuned as long as frequency and phase of the signals at both inputs are the same. The frequency of the VCO signal is divided by a pre-divider with selectable ratio (S 89) and by the two synchronous dividers A and B of IC S 187. Thus a frequency, being in the magnitude of the reference frequency, is generated. The synchronous dividers are programmed via the diode matrix S 353 at inputs A_1 to A_{64} and B_1 to B_{256} (active "high").

There is the following relation between reference frequency and VCO frequency:

$$\frac{f_{VCO}}{f_{ref.}} = (Q - P) \times a + P \times b \quad (1)$$

whereas:

a = ratio of synchronous divider A

b = ratio of synchronous divider B

P = ratio = 100 (of the pre-divider)

Q = ratio = 101 (of the pre-divider)

$f_{ref.} = (3.2 \text{ MHz} \div 640) = 5 \text{ kHz}$

With the stated values for P and Q it follows:

$$f_{VCO} = (a + 100 \times b) \times 5 \text{ kHz} \quad (2)$$

As it is obvious from the above equation the frequency f_{VCO} is increased by 5 kHz if " a " is raised by 1 and increased by 500 kHz if " b " is raised by 1.

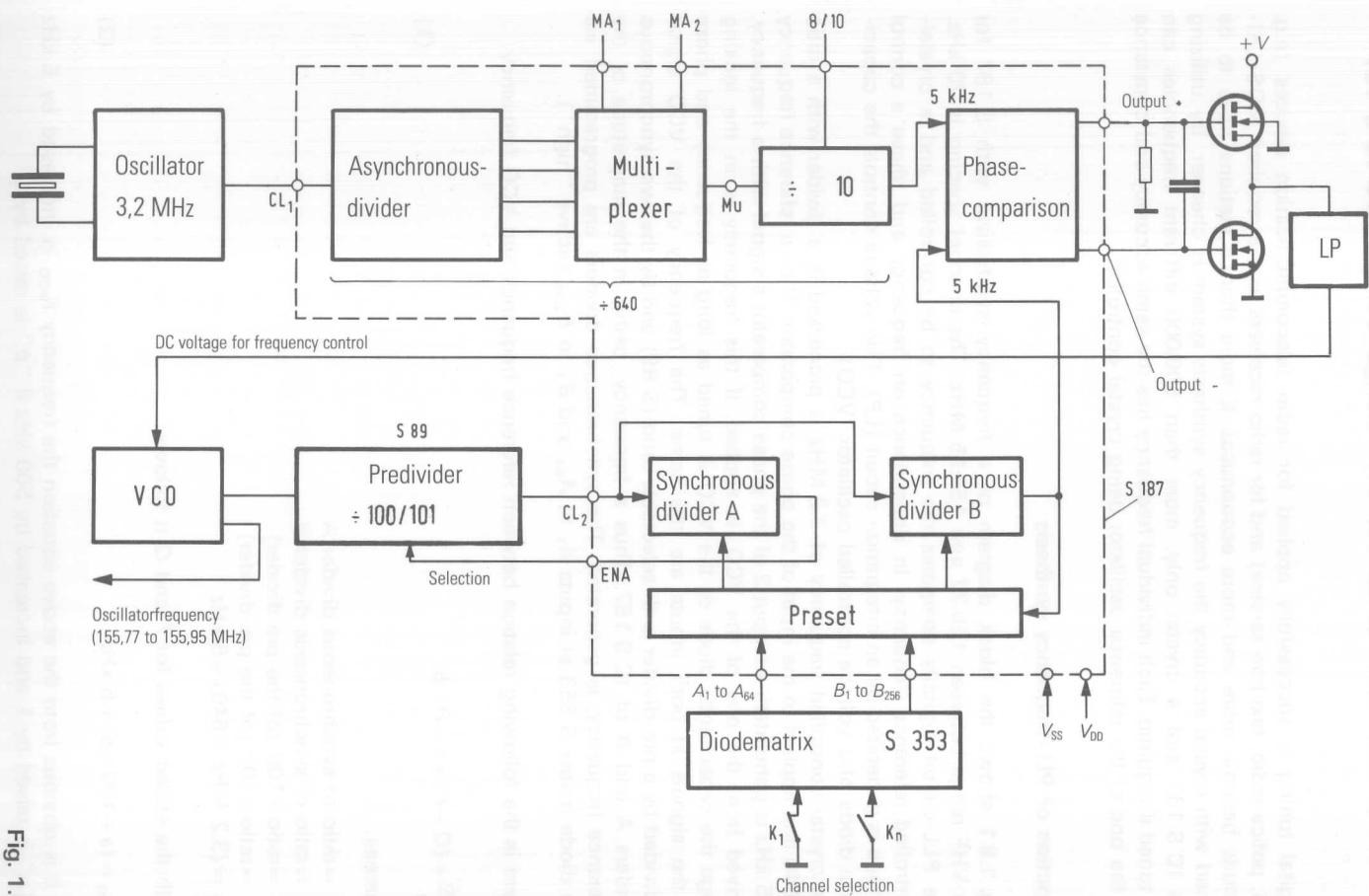


Fig. 1.6.1

The following table shows all VCO-frequencies which can be generated by varying the ratio of the synchronous dividers A and B. Besides that the table indicates the programming, being necessary for the diode matrix S 353. Programming conditions are stated in the data sheet for this IC.

Fre- quency	Divider		Programming of diode matrix																
MHz	A	B		A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}
155.770	54	311	E_1	X	0	X	0	X	X	0	X	X	X	0	X	X	0	0	X
155.790	58	311	E_2	0	X	X	0	X	X	0	X	X	X	0	X	X	0	0	X
155.810	62	311	E_3	X	X	X	0	X	X	0	X	X	X	0	X	X	0	0	X
155.830	66	311	E_4	0	0	X	0	0	0	X	X	X	X	0	X	X	0	0	X
155.850	70	311	E_5	X	0	X	0	0	0	X	X	X	X	0	X	X	0	0	X
155.870	74	311	E_6	0	X	X	0	0	0	X	X	X	X	0	X	X	0	0	X
155.890	78	311	E_7	X	X	X	0	0	0	X	X	X	X	0	X	X	0	0	X
155.910	82	311	E_8	0	0	X	0	X	0	X	X	X	X	0	X	X	0	0	X
155.930	86	311	E_9	X	0	X	0	X	0	X	X	X	X	0	X	X	0	0	X
155.950	90	311	E_{10}	0	X	X	0	X	0	X	X	X	X	0	X	X	0	0	X

X=non-conductive diode

The matrix outputs A_8 to A_{16} are not changed when the 10 channels are set (E_1 to E_{10}) because the ratio of divider B is not varied.

Operational function

Fig. 1.6.2 shows the complete circuit of the frequency synthesizer for the VHF range $f=155.77$ to 155.95 MHz. The supply voltage is 10 V. For the pre-divider a supply voltage of 5 V is additionally required.

The 3.2 MHz-signal is generated in a crystal-controlled oscillator circuit with BC 238 B. The frequency is accurately tuned by the variable capacitor C_2 (10 to 40 pF). In the following stage with BSY 62 A the signal is amplified and applied to the input CL_1 of the PLL-device with a necessary amplitude of approx. 10 V_{pp}.

The voltage-controlled oscillator consists of a circuit with capacitive feedback and with transistor BF 606 A. This pnp-transistor offers the advantage in that the collector can be directly connected to ground via the tuned circuit. The required frequency tuning is realized by the capacitance diode BB 505 G. The individual channel frequencies are generated by varying the tuning voltage V_R in a range between 4.6 and 5.1 V. The VCO-output is weakly coupled to the following frequency divider S 89, operating accordingly to the modulo-N-principle ($V_E \geq 50 V_{r.m.s.}$). It divides the frequency by a factor of 100 or 101 and supplies the adequate signal to the PLL-device.

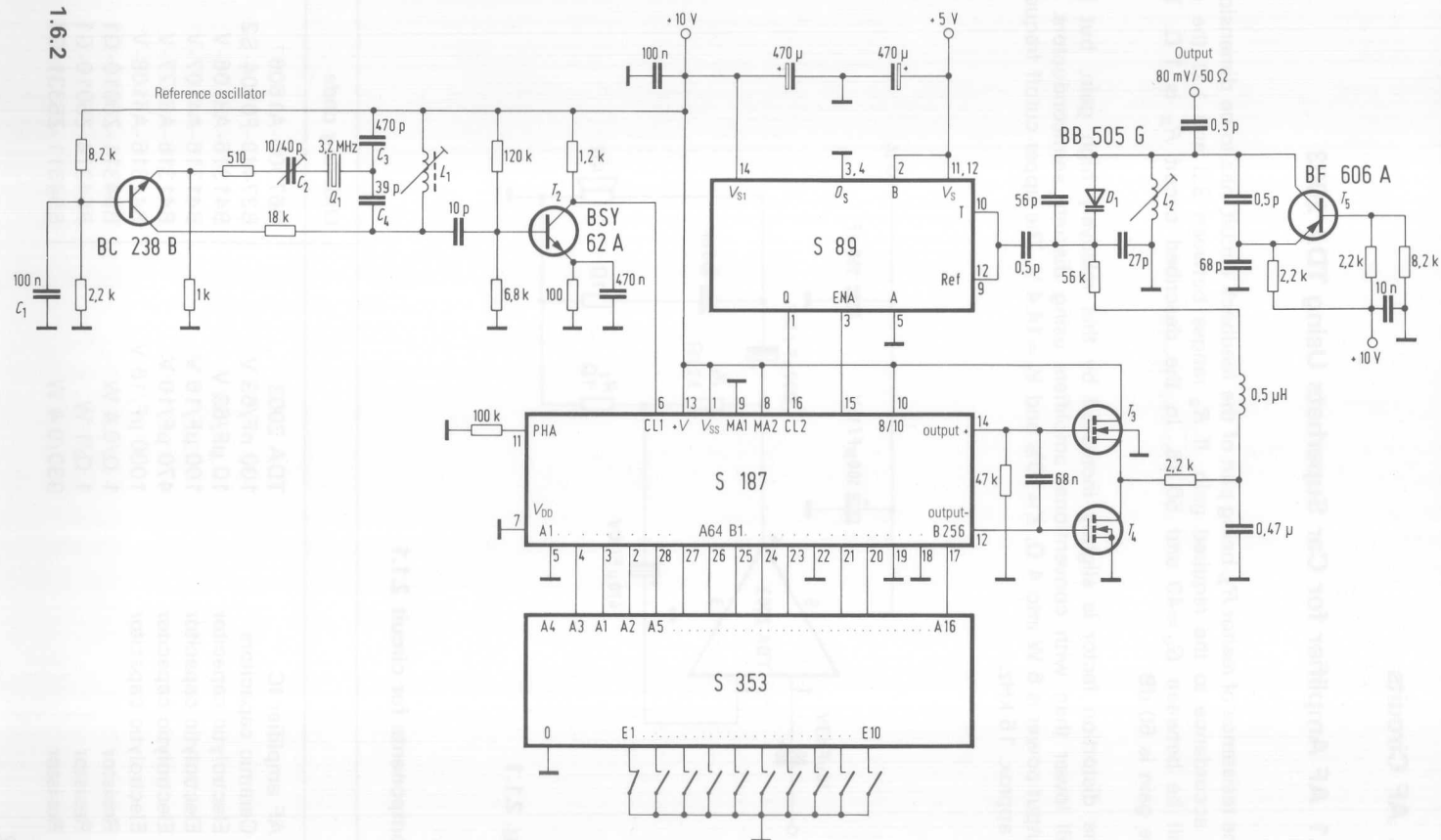
The control pulses being available at the output of the phase comparator are supplied via the n-channel MOS-transistors T_4 and T_5 to the low-pass filter consisting of the passive components R_{15} and C_{18} . As this filter operates like an integrator a pure dc voltage is available at its output. This dc voltage is applied to the capacitance diode D_1 and tunes the VCO, the frequency of which features the same accuracy as a crystal.

The lay-out of the frequency synthesizer is not critical. But it has to be considered that the pulse generating circuit does not influence the VCO. Therefore the lines and even the ground line have to be carefully separated on the pc board.

Components for circuit 1.6

		Ordering code
1 IC	S 89	Q67000-H1694
1 IC	S 187	Q67100-Y199
1 IC	S 353	Q67000-R109
2 FET N-channel (automatic locking)		proto types
1 Transistor	BC 238 B	Q62702-C279
1 Transistor	BSY 62 A	Q60218-Y62-A
1 Transistor	BF 606 A	Q62702-F535
1 Diode	BB 505 G	Q62702-B115
1 Crystal	3200 kHz	—
3 Ceramic capacitors	0.5 pF/500 V	B38182-A5000-C502
1 Ceramic capacitor	10 pF/63 V	B38062-A6100-G6
1 Ceramic capacitor	27 pF/63 V	B38062-J6270-G6
1 Ceramic capacitor	39 pF/63 V	B38066-J6390-G6
1 Ceramic capacitor	56 pF/63 V	B38066-J6560-G6
1 Ceramic capacitor	68 pF/63 V	B38066-J6680-G6
1 Ceramic capacitor	470 pF/63 V	B37062-A6471-K6
1 MKT-capacitor	10 nF/63 V	B32509-C103-M
1 MKT-capacitor	68 nF/63 V	B32509-C683-M
2 MKT-capacitors	100 nF/63 V	B32509-C104-M
2 MKT-capacitors	470 nF/100 V	B32560-D1474-J
2 Electrolytic capacitors	470 μ F/16 V	B41286-A4477-T
1 Oscillator coil L_1 (Fa. Toko)		YXNS30931X
1 Oscillator coil (air coil)		—
3 turns, 3,5 mm $\varnothing$, CuAG, 0.8 mm		—
RF choke, 0.5 μ H (air coil)		—
1 Resistor	100 Ω /0.5 W	B51261-Z4101-J1
1 Resistor	510 Ω /1 W	B51276-A2511-G
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	1.2 k Ω /0.5 W	B51261-Z4122-J1
4 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
2 Resistors	8.2 k Ω /0.5 W	B51261-Z4822-J1
1 Resistor	6.8 k Ω /0.5 W	B51261-Z4682-J1
1 Resistor	18 k Ω /0.5 W	B51261-Z4183-J1
1 Resistor	47 k Ω /0.5 W	B51261-Z4473-J1
1 Resistor	56 k Ω /0.5 W	B51261-Z4563-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	120 k Ω /0.5 W	B51261-Z4124-J1

Fig. 1.6.2



2. AF Circuits

2.1 AF Amplifier for Car Superhets Using TDA 2003

The resistance of resistor R_2 , being part of the feedback circuit, has to be dimensioned in accordance to the required gain. If R_2 ranges between 3.3 and 1 Ω the gain will be between $G_U=40$ and 50 dB. In the described circuit R_2 is 1 Ω . Thus the gain is 50 dB.

The distortion factor is slightly increased by this relatively high gain, but it is still lower than with conventional amplifiers using discrete semiconductors. The output power is 6 W into 4 Ω , $K=10\%$ and $V_s=14.4$ V. The upper cutoff frequency is approx. 15 kHz.

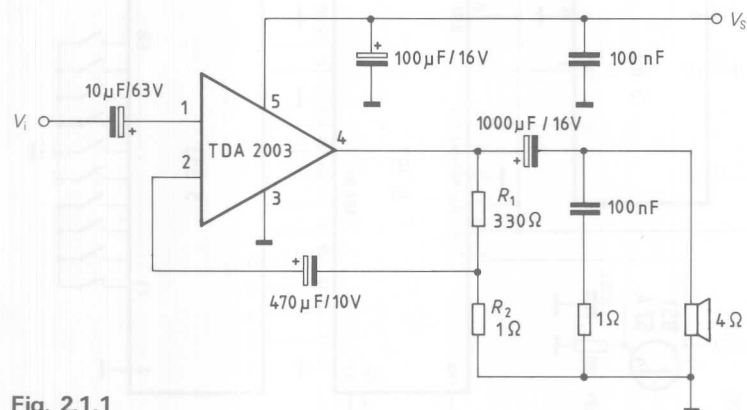


Fig. 2.1.1

Components for circuit 2.1.1

		Ordering code
1 AF amplifier IC	TDA 2003	Q67000-A1606
2 Ceramic capacitors	100 nF/63 V	B37449-F6104-S2
1 Electrolytic capacitor	10 μF/63 V	B41316-A8106-V
1 Electrolytic capacitor	100 μF/16 V	B41316-A4107-V
1 Electrolytic capacitor	470 μF/10 V	B41316-A3477-V
1 Electrolytic capacitor	1000 μF/16 V	B41316-A4108-V
1 Resistor	1 Ω /0.4 W	B54311-Z5010-G1
1 Resistor	1 Ω /1 W	B54314-Z5010-G1
1 Resistor	330/0.4 W	B54311-Z5331-G1

Fig. 2.1.2 shows a bridge amplifier using two TDA 2003. By this circuit an output power of 20 W into 4 Ω is realized. The distortion factor K is 10% and the power-supply voltage V_s is 14.6 V. The advantage of this circuit is in that an additional electrolytic output capacitor is not required.

The gain of the circuit can be calculated as follows:

$$G_U = \frac{4 \times R_1}{R_2} \text{ with } R_3 \approx 2 \times R_1$$

With the resistances indicated in the circuit of fig. 2.1.2 a gain of 34 dB ($\approx$ 48-fold) is obtained. The resulting cutoff frequency is approx. 50 kHz.

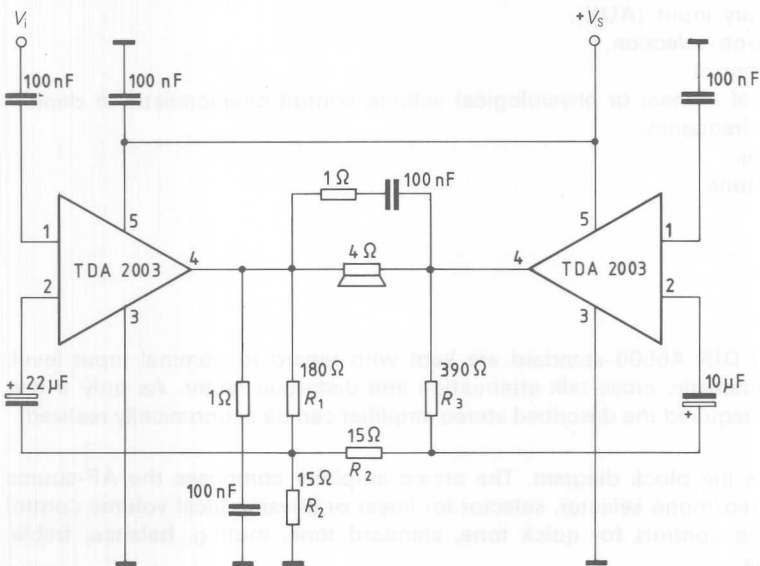


Fig. 2.1.2

Components for circuit 2.1.2

		Ordering code
1	AF amplifier IC	TDA 2003
5	Ceramic capacitors	100 nF/63 V
1	Electrolytic capacitor	10 μF/63 V
1	Electrolytic capacitor	22 μF/63 V
2	Resistors	1 Ω/1 W
2	Resistors	15 Ω/0.5 W
1	Resistor	180 Ω/0.5 W
1	Resistor	390 Ω/0.5 W
		Q67000-A1606
		B37449-F6104-S2
		B41316-A8106-V
		B41316-A8226-V
		B54314-Z5010-G1
		B51261-Z4150-J1
		B51261-Z4181-J1
		B51261-Z4391-J1

2.2 Digitally Controlled Stereo Amplifier with IR Remote Control

Generally a great engineering effort is necessary to realize a wireless controlled stereo amplifier. But with the increasing application of integrated circuits and microcomputers the elaborateness of components has been drastically reduced. If the IC TDA 4290 is used the control devices can be installed at any place of the front-panel without using screened AF-lines. TDA 4290 is provided for DC control of volume, treble, bass and balance.

Remote control of the following operations is possible.

- 1st AF-source selection for record player (TA), tape recorder (TB), tuner (TU) and auxiliary input (AUX),
- 2nd Stereo/mono-selection,
- 3rd Volume control,
- 4th Selection of a linear or physiological volume control characteristic in dependence on frequency,
- 5th Quick tone,
- 6th Standard tone,
- 7th Muting,
- 8th Balance,
- 9th Treble,
- 10th Bass.

Requirements of DIN 45500-standard are kept with regard to nominal input level, frequency characteristic, cross-talk attenuation and distortion factor. As only a few components are required the described stereo amplifier can be economically realized.

Fig. 2.2.1 shows the block diagram. The stereo amplifier comprises the AF-source selector, the stereo/mono selector, selector for linear or physiological volume control characteristic, the controls for quick tone, standard tone, muting, balance, treble, bass and volume.

An equalizing preamplifier is provided for magnetic phono pickups. The push-pull output amplifiers operate with two 15 W-power-amplifier ICs each.

The digital control information is available either from a microcomputer controlled system or from an IR remote control system. It is applied to the stereo preamplifier SV 79 via the MOS IC SAB 4209 (receiver of IR remote control system). SV 79 supplies the analog signals for volume, bass, treble and balance control. The control is indicated by LEDs operated by the LED-driving IC UAA 180.

The block diagram of SV 79 is shown in fig. 2.2.2.

The selection of the four stereo input sources TA, TB, TU and AUX is electronically realized by the IC TDA 1195 when the digital control signals are applied to pins 30, 32, 34 and 35. The following table shows the reaction of the control signals.

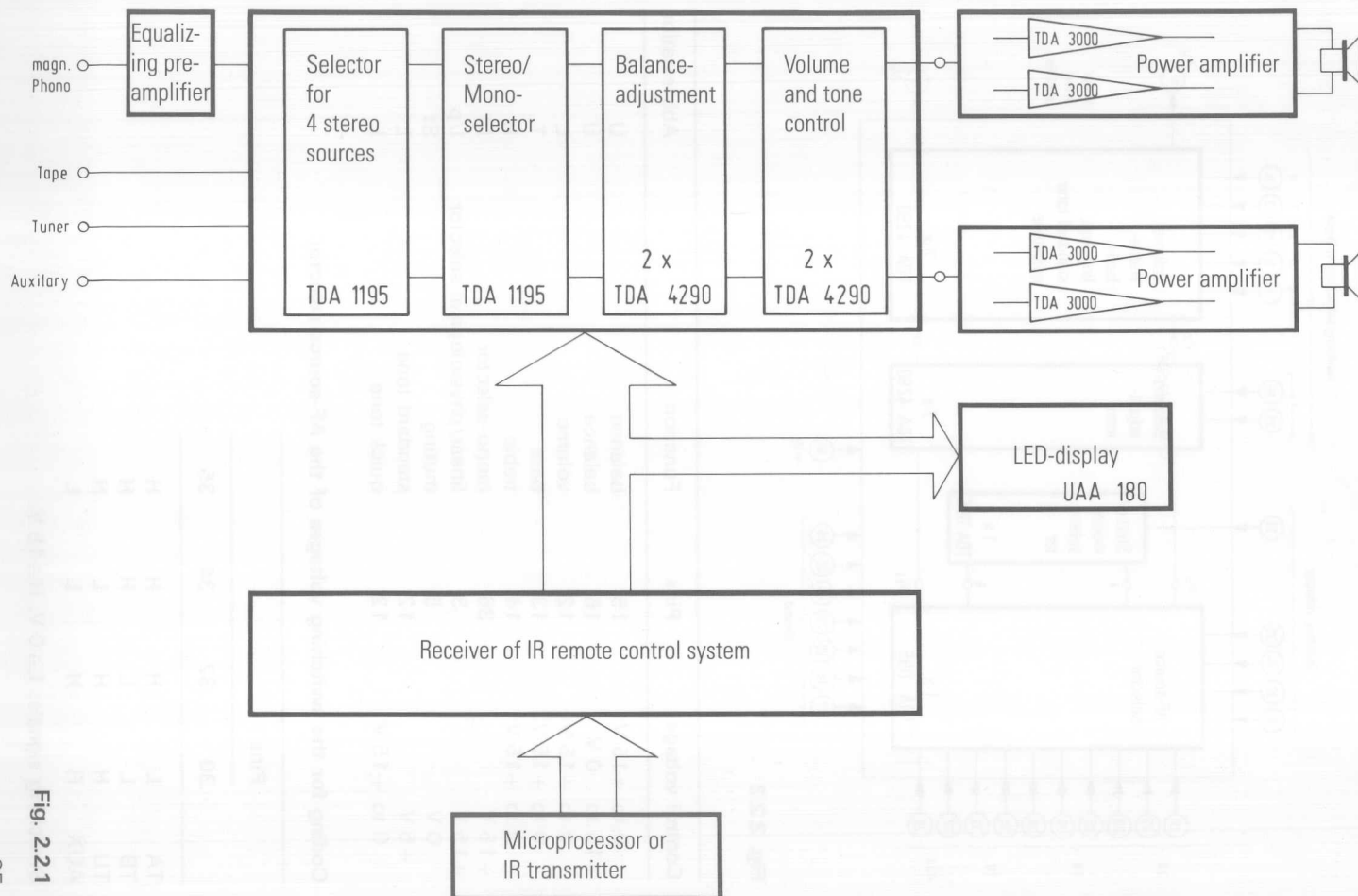


Fig. 2.2.1

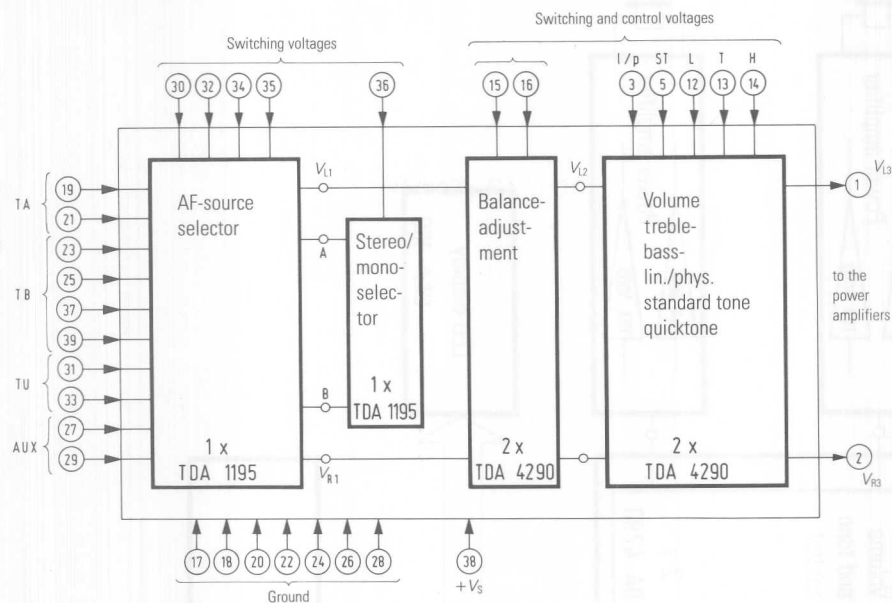


Fig. 2.2.2

Control voltage	Pins	Function	Abbreviation
0 to +15 V	15	balance	U
+15 to 0 V	16	balance	$\bar{U}$
0 to +15 V	12	volume	L
0 to +15 V	13	bass	T
0 to +15 V	14	treble	H
+15 V	36	mono-selector	M
+15 V	3	linear/physiological selector	I/p
0 V	5	muting	St
+5 V	12	standard tone	L
0 to +15 V	12	quick tone	L

Coding for the switching voltages of the AF-source selector

		Pins			
		30	32	34	35
TA	L	H	H	H	H
TB	L	L	H	H	H
TU	H	H	L	H	H
AUX	H	H	L	L	L

Switching signals: L $\leq$ 0 V, H $\geq$ 15 V.

The total circuit for AF-source selection is shown in **fig. 2.2.3**.

The supply voltage of $0.5 \times V_s$ required for the IC TDA 1195 is generated by a high-resistance voltage divider of the following common-emitter-circuit. Its low output impedance guarantees a matching optimum for the following balance circuit. Another common-emitter-circuit eliminates retroactions from the TB-output.

Outputs A and B of the AF-source selector are connected to the stereo/mono-selector TDA 1195. Mono-operation is obtained by applying a signal with H-level to the control input (pin 36, see also **fig. 2.2.2**). In this case both outputs are connected in parallel. **Fig. 2.2.4** shows a circuit with the IC TDA 1195.

Balance adjustment of the AF signals is realized by two ICs, type TDA 4290, with linear volume control characteristics as shown in **fig. 2.2.5**. The adjustment signal is applied to pin 5 of each TDA 4290. The required set-signals are generated as follows. The digital signal being controlled by the pulse duty factor and supplied from the IR remote control receiver SAB 4209 is processed by an inverter.

Both inverted and non-inverted signals are integrated by two RC-circuits having exactly the same time constant. They are available as oppositely oriented dc voltages for the balance adjustment ICs (refer to **fig. 2.2.6**).

The adjustment is dimensioned in that the signal of the second channel is increased by +4 dB and kept constant when the level of the first channel is attenuated to zero. Therefore the middle of the balance range is -4 dB below the signal maximum.

The circuit for volume control with physiological characteristic is shown in **fig. 2.2.7**.

IC TDA 4290 essentially includes four operational amplifiers with so-called electronic potentiometers. For volume control with physiological characteristic the outputs of two operational amplifiers are connected in parallel via an RC-circuit. By selecting a different attenuation characteristic of these electronic potentiometers a physiological frequency characteristic in dependence on volume control is obtained by the RC-circuit. If an equal attenuation characteristic (linear operation) is selected this correction of the frequency characteristic is ineffective. The selection of physiological or linear volume control is realized by applying an L-signal to pin 3 (see **fig. 2.2.7**). If paired ICs of type TDA 4290 are used the volume control for both channels differs not more than ± 0.5 dB.

The two other operational amplifiers also operate as electronic potentiometers. They control treble and bass by adjustment voltages applied to pin 13 and 14. In this case a minimum of external components is required, i.e. only a capacitor each. The variation range within the adjustment limits is 32 dB at test frequencies of 40 Hz and 15 kHz. A linear characteristic is achieved at half of the adjustment voltage.

The output amplifier consists of two stages with two push-pull 15 W-AF-amplifier ICs, type TDA 3000, each. The circuit is shown in **fig. 2.2.8**. Because of this

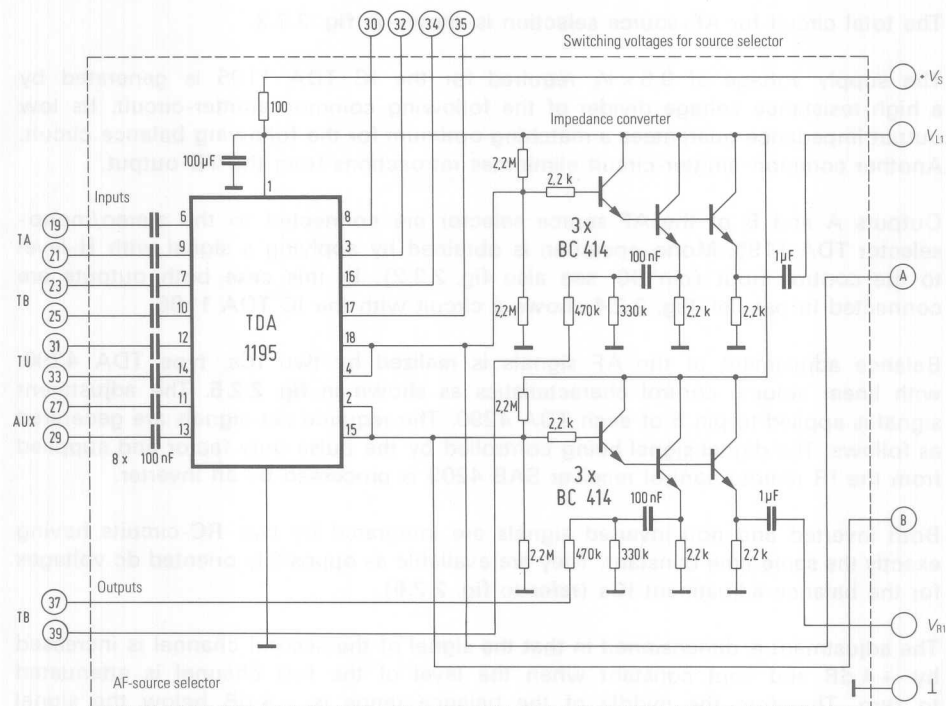


Fig. 2.2.3

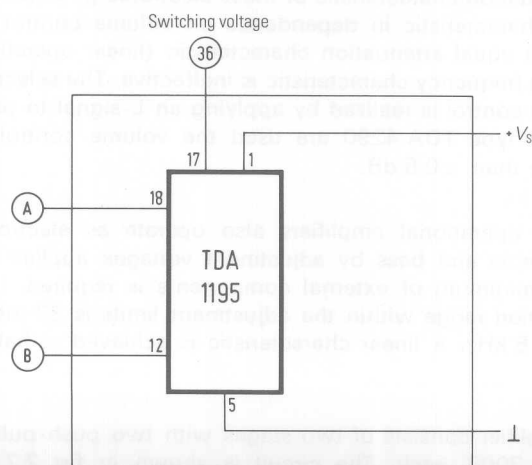


Fig. 2.2.4

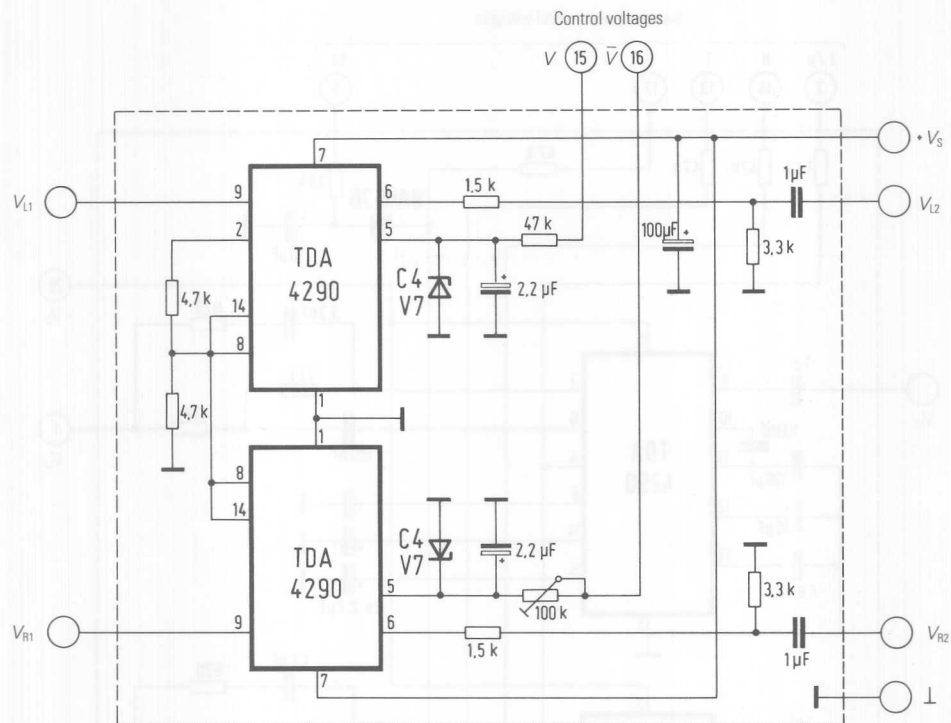


Fig. 2.2.5

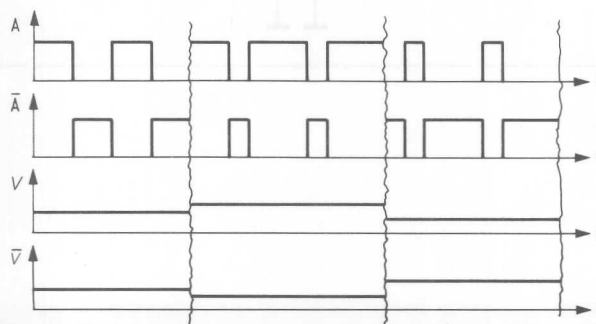


Fig. 2.2.6

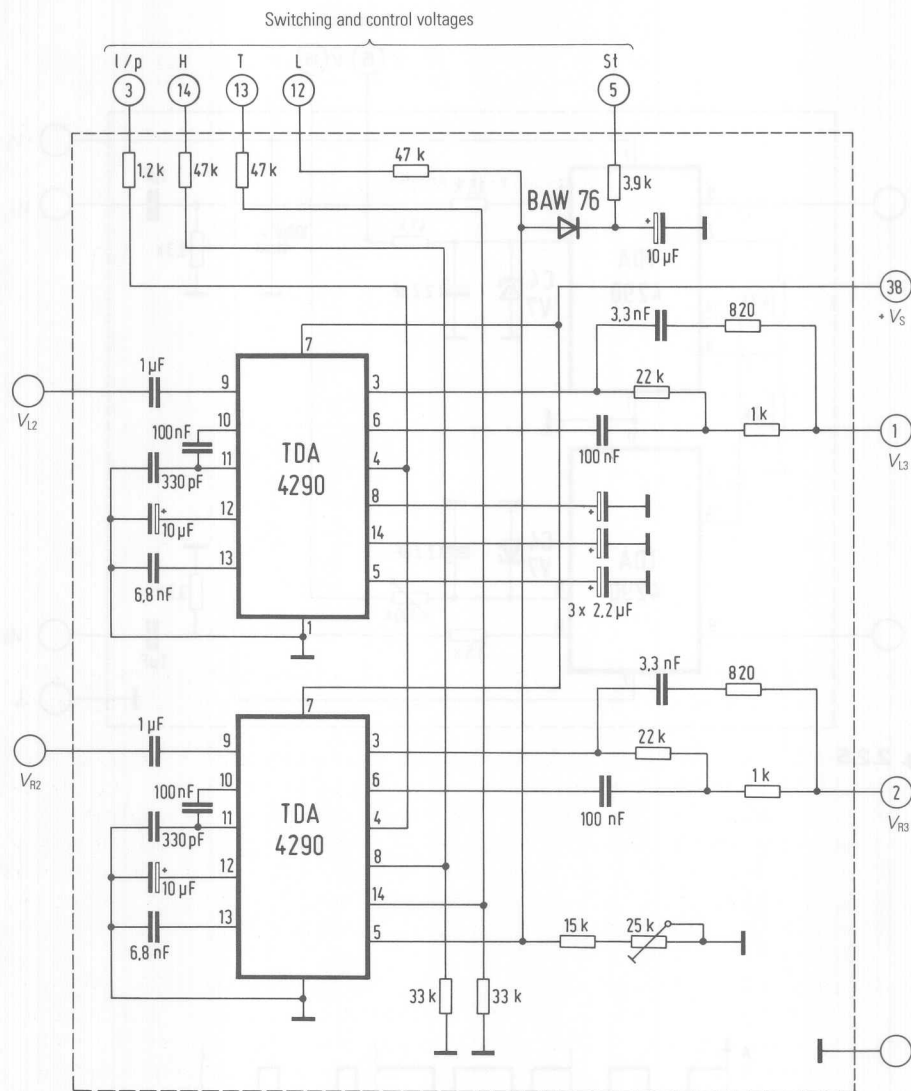


Fig. 2.2.7

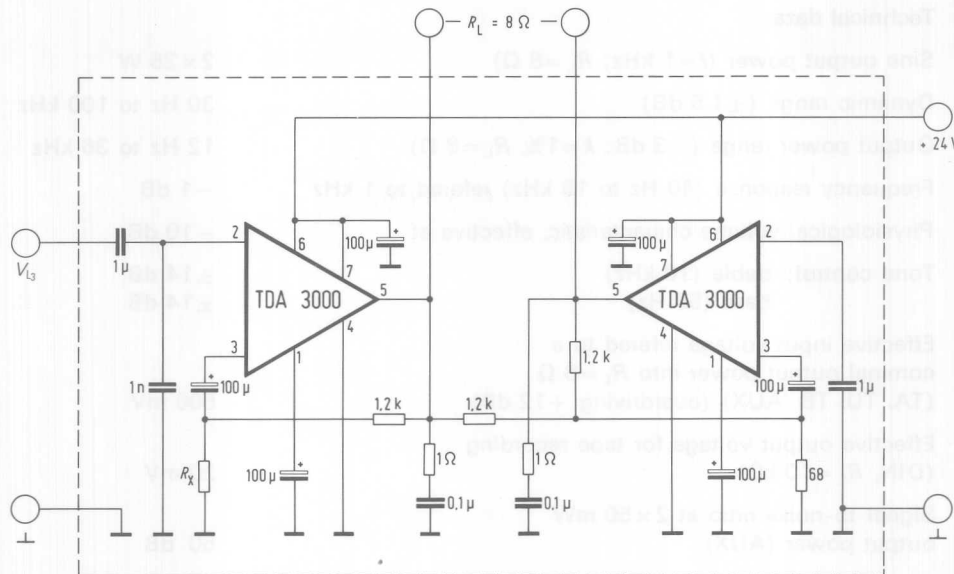


Fig. 2.2.8

push-pull operation an output power, being 4 times greater than that of amplifiers with push-pull arrangement and A-mode operation or with simple B-mode operation.

Both amplifier ICs are simultaneously operated, but their output voltages are dephased by 180° . As the load resistor is connected between the two outputs the voltage drop across this resistor is twice higher than at single operation with reference to ground (B-mode output stage). The phase shift of the output voltage of IC₂ is attained by utilizing the inverted input at pin 3. The gain is adjustable at IC₁. The difference of both output voltages should be as small as possible to avoid undesired power losses at the integrated circuits and at the load resistor.

Each output stage operates either with two ICs, type TDA 2870, preferably running at $V_s \leq 18\text{ V}$, or with two TDA 3000 operated at $V_s \leq 26\text{ V}$. As these ICs have a very low residual voltage a high output power is possible. The voltage gain is adjustable by the feedback resistor R_x . As only a few external components are required for the ICs the output power stage can be economically realized. This also applies to the power supply, as only a supply voltage is necessary.

In fig. 2.2.9 the total circuit of the stereo amplifier is shown.

Technical data:

Sine output power ($f=1$ kHz; $R_L=8\ \Omega$)	2×25 W
Dynamic range (± 1.5 dB)	30 Hz to 100 kHz
Output power range (-3 dB; $k=1\%$, $R_L=8\ \Omega$)	12 Hz to 36 kHz
Frequency response (40 Hz to 16 kHz) referred to 1 kHz	-1 dB
Physiological volume characteristic, effective at	-10 dB
Tone control: treble (10 kHz)	± 14 dB
bass (50 Hz)	± 14 dB
Effective input voltage referred to a nominal output power into $R_L=8\ \Omega$ (TA, TU, TB, AUX) (overdriving $+12$ dB)	500 mV
Effective output voltage for tape recording (DIN, $R_L=10$ k Ω)	20 mV
Signal-to-noise ratio at 2×50 mW output power (AUX)	50 dB
Distortion factor ($f_{in}=1$ kHz, $P_{out}=25$ W, $R_L=8\ \Omega$)	0.3%
Cross-talk attenuation between the two stereo channels, $f_{in}=1$ kHz	48 dB
Between two input channels	
AUX – TB	46 dB
$f_{in}=1$ kHz, AUX – TA	56 dB
AUX – TU	48 dB

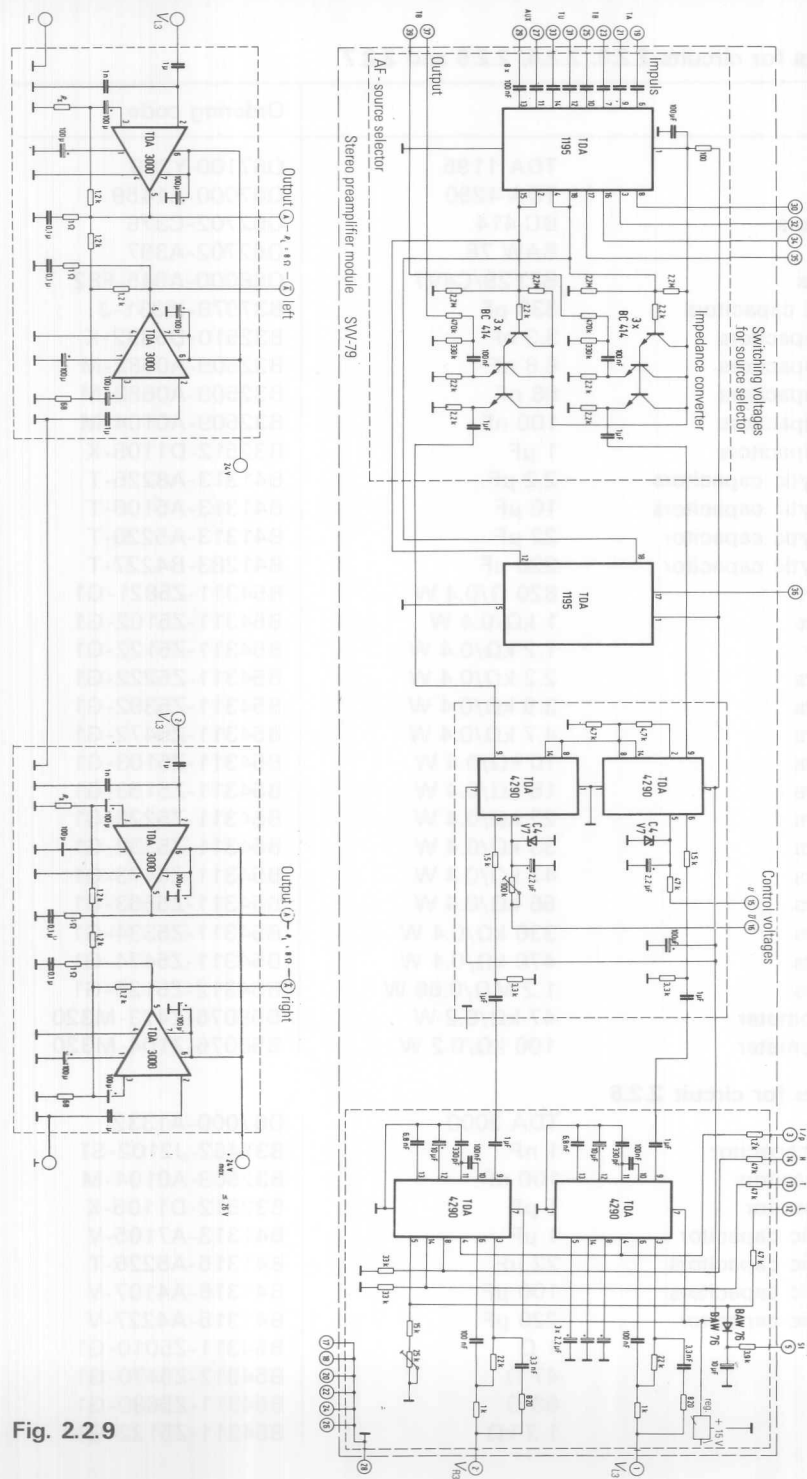


Fig. 2.2.9

Components for circuits 2.2.3, 2.2.4, 2.2.5 and 2.2.7

		Ordering code
2 ICs	TDA 1195	Q67100-Y389
4 ICs	TDA 4290	Q67000-A1459
6 Transistors	BC 414	Q62702-C376
1 Diode	BAW 76	Q62702-A397
2 Z-diodes	BZY29/C4V7	Q68000-A945-F82
2 Ceramic capacitors	330 pF	B37979-I5331-J
2 MKT-capacitors	3.3 nF	B32510-D6332-K
2 MKT-capacitors	6.8 nF	B32509-A0682-M
2 MKT-capacitors	68 nF	B32509-A0683-M
13 MKT-capacitors	100 nF	B32509-A0104-M
4 MKT-capacitors	1 μ F	B32512-D1105-K
7 Electrolytic capacitors	2.2 μ F	B41313-A8225-T
2 Electrolytic capacitors	10 μ F	B41313-A5106-T
1 Electrolytic capacitor	22 μ F	B41313-A5226-T
1 Electrolytic capacitor	220 μ F	B41283-B4227-T
2 Resistors	820 Ω /0.4 W	B54311-Z5821-G1
8 Resistors	1 k Ω /0.4 W	B54311-Z5102-G1
1 Resistor	1.2 k Ω /0.4 W	B54311-Z5122-G1
4 Resistors	2.2 k Ω /0.4 W	B54311-Z5222-G1
2 Resistors	3.9 k Ω /0.4 W	B54311-Z5392-G1
2 Resistors	4.7 k Ω /0.4 W	B54311-Z5472-G1
3 Resistors	10 k Ω /0.4 W	B54311-Z5103-G1
2 Resistors	15 k Ω /0.4 W	B54311-Z5153-G1
2 Resistors	22 k Ω /0.4 W	B54311-Z5223-G1
2 Resistors	33 k Ω /0.4 W	B54311-Z5333-G1
5 Resistors	47 k Ω /0.4 W	B54311-Z5473-G1
3 Resistors	56 k Ω /0.4 W	B54311-Z5563-G1
2 Resistors	330 k Ω /0.4 W	B54311-Z5334-G1
2 Resistors	470 k Ω /0.4 W	B54311-Z5474-G1
4 Resistors	1.2 M Ω /0.66 W	B54312-Z5125-G1
1 Potentiometer	47 k Ω /0.2 W	B58076-Z473-M320
1 Potentiometer	100 k Ω /0.2 W	B58076-Z104-M320

Components for circuit 2.2.8

2 ICs	TDA 3000	Q67000-A1332
1 Ceramic capacitor	1 nF	B37462-J2102-S1
2 MKT-capacitors	100 nF	B32509-A0104-M
1 MKT-capacitor	1 μ F	B32512-D1105-K
1 Electrolytic capacitor	1 μ F	B41313-A7105-V
2 Electrolytic capacitors	22 μ F	B41315-A5226-T
3 Electrolytic capacitors	100 μ F	B41316-A4107-V
1 Electrolytic capacitor	220 μ F	B41316-A4227-V
2 Resistors	1 Ω	B54311-Z5010-G1
1 Resistor	47 Ω	B54312-Z5470-G1
1 Resistor	68 Ω	B54311-Z5680-G1
3 Resistors	1.2 k Ω	B54311-Z5122-G1

2.3 Two-Channel PCM-Codec for Digital Telephone Switching Systems

Small private branch exchange systems usually operate with electronic crosspoint switches making through-connections for the transmission of analog speech-band signals. However, greater exchange systems, covering a very large number of lines, advantageously employ digital crosspoint networks, as they can be efficiently and economically realized by integrated circuits and memory devices.

With digital systems only digitized signals are through-connected by the crosspoint networks. Therefore all installations for subscriber sets and for operating other exchange systems have to be individually provided for. For analog subscriber sets these performances are as follows: subscriber line interface circuit (SLIC), transmitter and receiver filter as well as coders and decoders (CODEC).

The total Codec concept has been developed with the understanding in that both the complex digital functions and the extremely-accurate analog functions can be reliably realized on a minimum silicon chip size by using modern integration technologies. Therefore two different chips are used. They are economically produced in a technology which guarantees extremely reliable devices. As both chips are encapsulated in a 28 pin case, the highest packing density of all known Codec solutions is obtained. Because of the dynamic requirements all components used for two channels are integrated on the chips. Therefore a small mounting area for a Codec function per channel is required on the subscriber module.

From the variety of A/D-converting concepts the principle of successive approximation is utilized for the Codec device, as it offers an compromise optimum between operating frequency and elaborateness of analog standards. The circuit of the two-channel Codec is shown in **fig. 2.3**.

The PCM-2-channel-Codec device, type SM 61 C, is most favourable for the application of a subscriber in a digital exchange system of any size. Transmitting and receiving PCM-words are bit-serially exchanged between multiplex line and Codec register by 2.048 Mbits/s. This exchange as well as the internal process of coding and decoding for two channels are operated by a clock of 2.048 MHz. The synchronization and thus the adequate exchange time for the two channels of the total system are determined by the negative edge of the $\overline{\text{INSY}}$ -pulse. The pulse duration has to be longer than a 2.048-MHz-cycle. A 125 μs -reference frame between two scannings of a channel consists of 32 time gates with 8×2.048 MHz-clock cycles each. The timing of all Codec operations is as follows.

- Exchange of the 8-bit-PCM-word for channel 1: PCM IN (SUB 1), PCM OUT (SUB 1),
- Output of the decoded analog signal from channel 1: A OUT 1,
- Balancing of comparator: AUT C,
- Scanning of the analog input signal from channel 2: A IN 2,
- Successive generation of the PCM-word for channel 2: a bit is for the polarity sign, 3 bits are for the segment, and 4 bits are for assignment in the segment,

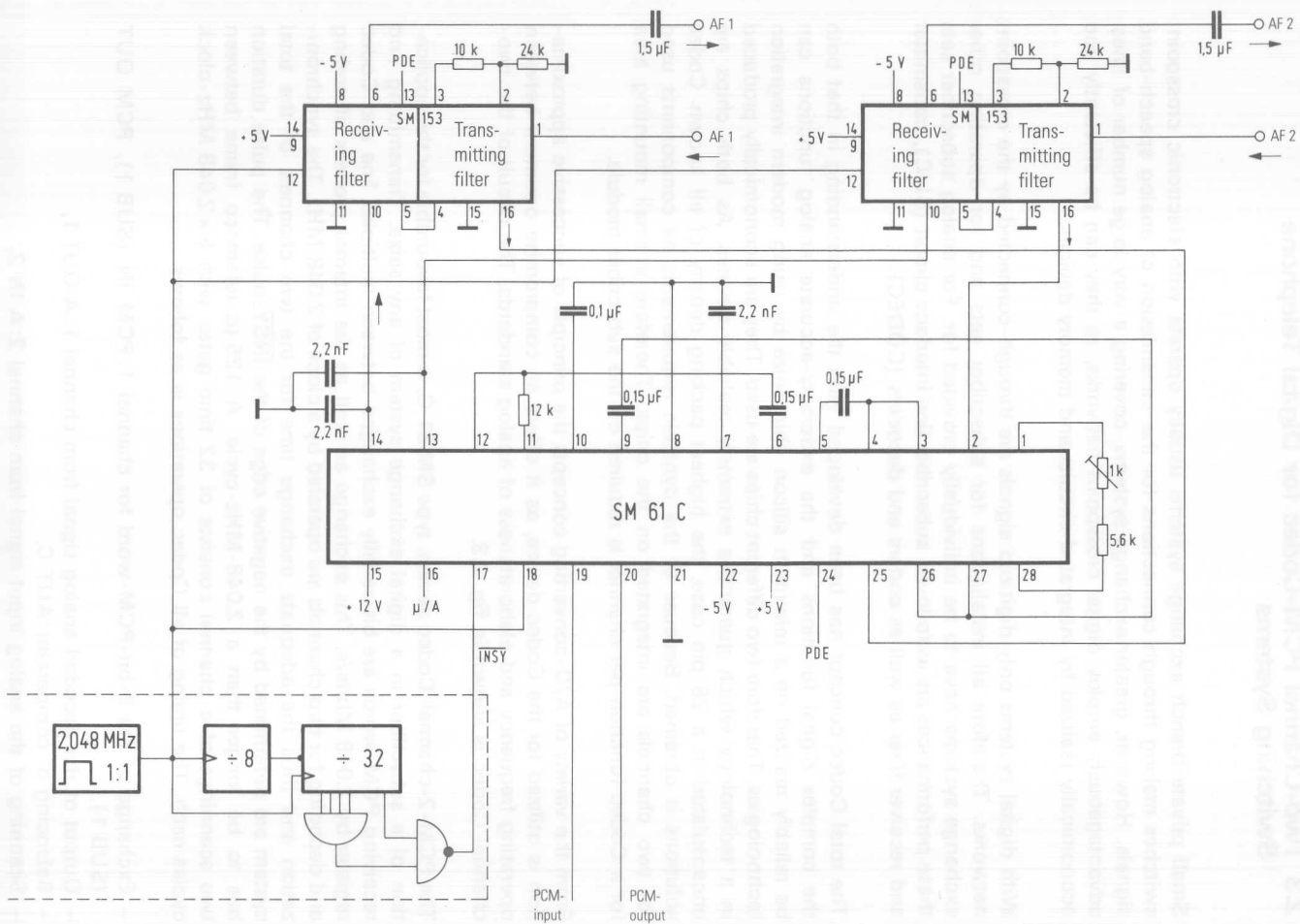


Fig. 2.3

- Exchange of the PCM-word for channel 2: PCM OUT (SUB 2), PCM IN (Sub 2),
- Output of the decoded analog signal from channel 2: A OUT 2,
- Balancing of the current-voltage-converter: OUT CV,
- Scanning of the analog input signal from channel 1: A IN 1,
- Generation of the PCM-word for channel 1.

Components for circuit 2.3

			Ordering code
1	2-channel PCM-CODEC	SM 61 C	Q67100-Z141
2	Receiver-transmitter filter	SM 153	Q67100-Y606
3	Polypropylene capacitors	2200 pF/160 V	B33063-B1222-H
2	MKT-capacitors	100 nF/63 V	B32509-A0104-M
1	MKT-capacitor	150 nF/63 V	B32509-A0154-M
2	MKT-capacitors	1.5 µF/100 V	B32512-D1155-K
1	Resistor	5.6 kΩ/0.5 W	B51261-Z4562-J1
2	Resistors	10 kΩ/0.5 W	B51261-Z4103-J1
1	Resistor	12 kΩ/0.5 W	B51261-Z4123-J1
2	Resistors	24 kΩ/0.5 W	B51261-Z4243-J1



3. TV Circuits

3.1 Siemens Digital Tuning System SDA 200

In **fig. 3.1.1** the block diagram of a digital tuning system is shown. It essentially consists of three major blocks:

Frequency processing,
Control and display,
Station memory.

The required frequencies are produced by a frequency synthesis generator operating accordingly to the phase-locked-loop principle. The PLL consists of a voltage controlled oscillator which is the tuner oscillator, a pre-divider, type SDA 2001, with a fixed ratio of 64:1, a programmable divider, type SDA 2002, and a phase comparator. The reference voltage for the latter is generated by a crystal oscillator with a frequency of 4 MHz and by a divider with the ratio of 2048:1. If the reference frequency of 1.93 kHz is multiplied by the divider ratio of SDA 2001, the result is 125 kHz ($=1.93 \text{ kHz} \times 64$) which is the smallest tuning step being possible.

The pre-divider manufactured in ECL-technology comprises two separate integrated preamplifiers, one for VHF the other for UHF. It has a fixed divider ratio of 64. The frequency maximum of the UHF input signal is 950 MHz. The sinusoidal input voltage should not be less than 300 mV at 470 MHz and 100 mV at 900 MHz. The minimum frequency of the VHF input signal is 60 MHz. The VHF input voltage

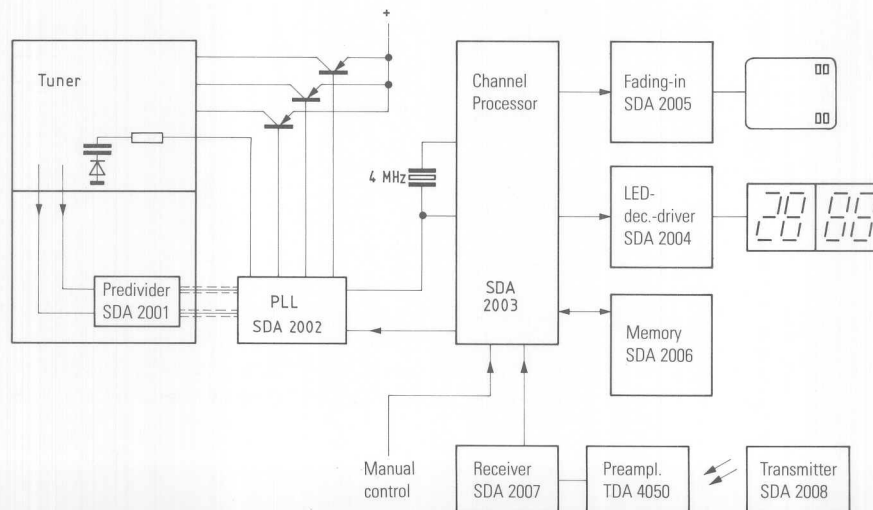
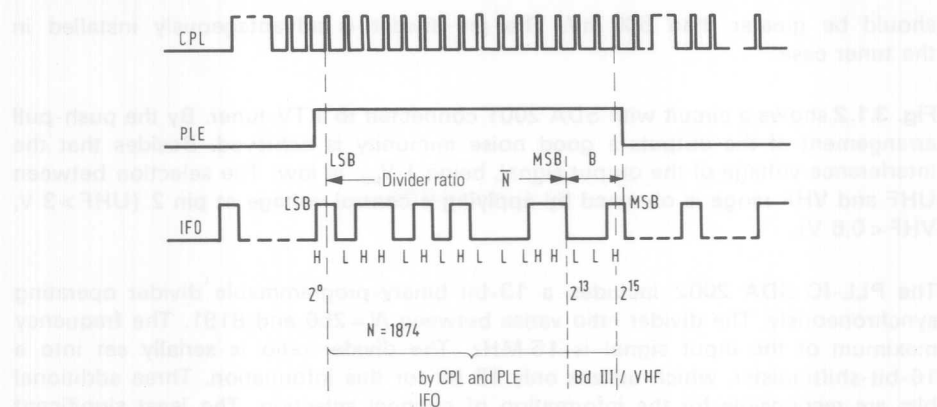


Fig. 3.1.1

Fig. 3.1.2 shows a circuit with SDA 2001 connected to a TV-tuner. By the push-pull arrangement of the outputs a good noise immunity is achieved. Besides that the interference voltage of the output signal, being $1 V_{pp}$, is low. The selection between UHF and VHF range is obtained by applying a control voltage at pin 2 (UHF $> 3 V$, VHF $< 0.6 V$).



Truth table for range selection

B						Range
Input "IFO" bit						
2 ¹³	2 ¹⁴	2 ¹⁵	B ₁	B ₂	B ₃	
H	H	H	H	H	L	UHF
H	L	H	H	L	H	Bd I / VHF
L	L	H	L	L	H	Bd III/ VHF
L	H	H	L	H	H	Cable channel

With positive logic the "IFO"-bits 2^0 to 2^{12} are complementary to the dual code of the dividing ratio N .

Fig. 3.1.3

A clock signal with the frequency of 62.5 kHz is available at the open-collector output CL (see fig. 3.1.4). The input of the synchronous divider: N is dimensioned for push-pull signals with ECL-level. If the PLL circuit is synchronized a signal with L-level is available at output LOCKIND. The phase detector can be operated by a separate supply voltage of $V_{S2} = 32$ V max. to obtain a tuning voltage of 30 V at output V_D . This voltage is required for the TV tuner.

The process of station tuning and storing the corresponding frequency information as well as the control of program or channel indication is coordinated by a single-chip microcomputer, type SDA 2003. It is connected between the programmable divider of the PLL-circuit and the electrically programmable memory, which stores the tuning information for the adequate channels. Therefore SDA 2003 is also named channel processor. It converts the tuning voltage to the corresponding frequency. The latter is a binary number which represents the divider ratio for the PLL divider. SDA 2003 serially supplies this information to the PLL-circuit SDA 2002 and to the decoder and display driver, type SDA 2004, for program and channel indication.

The data is transferred via the IFO-line being common for all external components. The assignment of the information to the responsible circuit is realized by three clock lines: clock channel (CKA), clock-PLL (CPLL) and clock program (CPR).

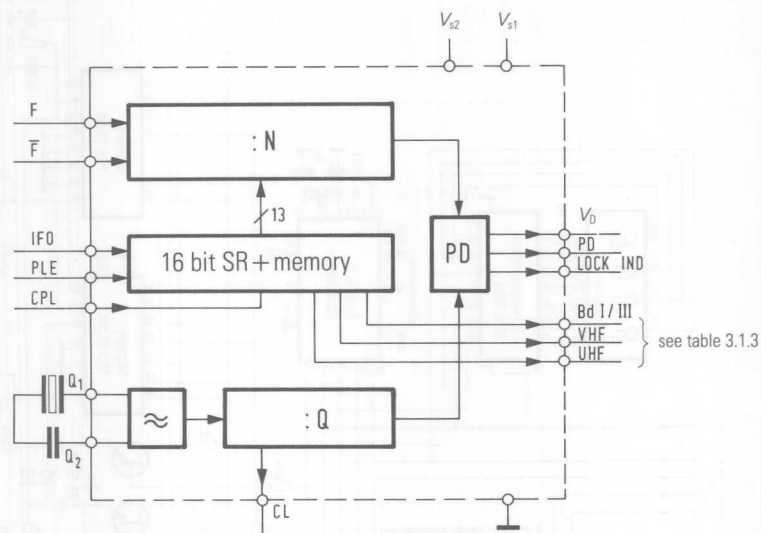
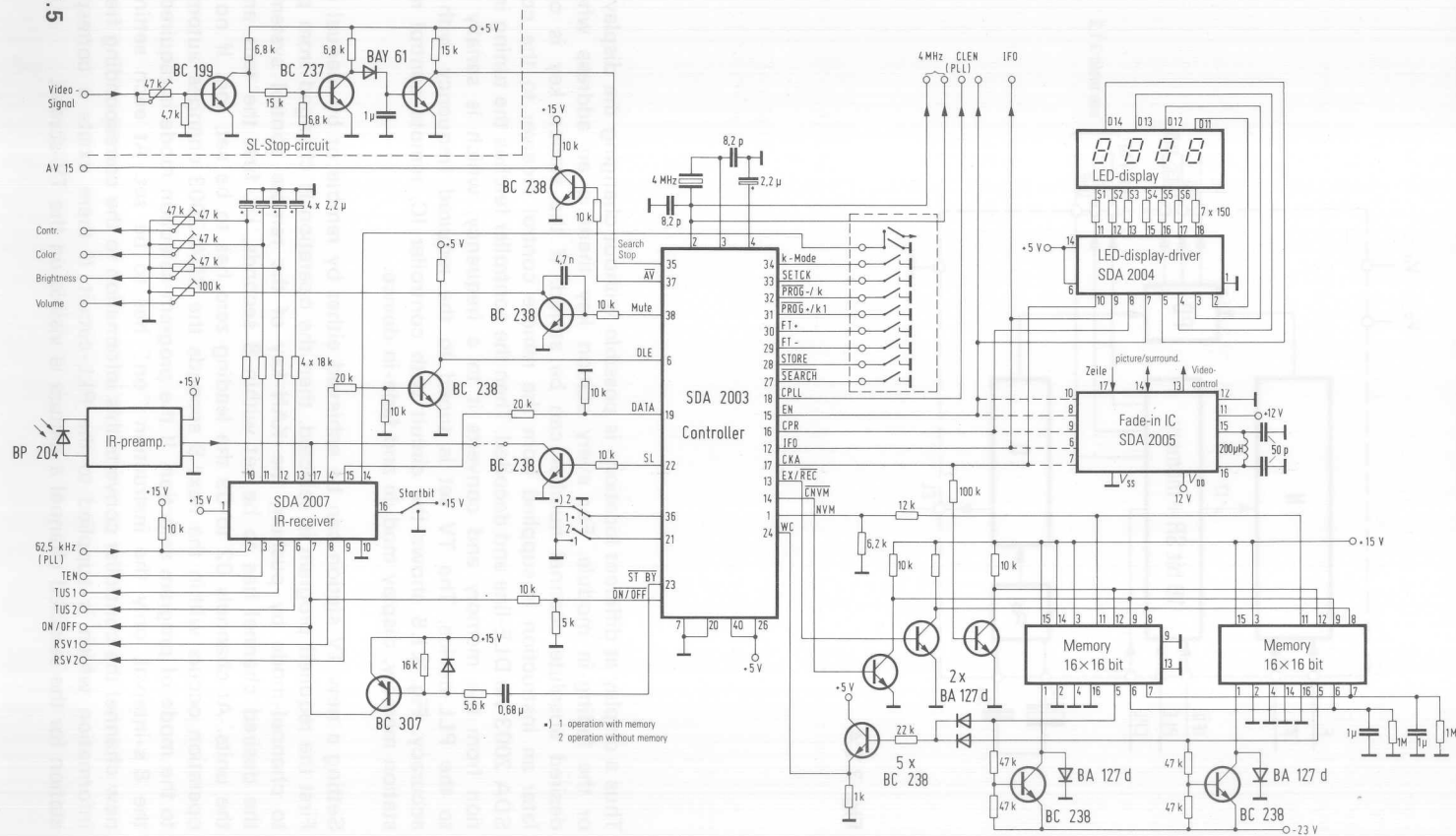


Fig. 3.1.4

Thus a display at different locations is possible without changing the display device or the fading-in module. For every station key there is an address where the desired absolute channel number can be stored. If the station key is operated later an instruction is supplied from the remote control receiver to the controller SDA 2003 via DLE-line and decoded. Then the controller fetches the tuning information from the memory and converts it to a frequency, which is serially applied to the PLL-device. The TV set is tuned to the required frequency with crystal accuracy. Fig. 3.1.5 shows the circuit with controller IC, remote control receiver, station memory, display module and fade-in device.

Setting a new TV station can be achieved either by remote or by manual control. First the required program is selected, then the operation is changed from program to channel-mode by pushing the KAN-key of the remote control system. Now the desired channel has to be set within 8 seconds, i.e. first the tens and then the units. At channels 02 to 09 the leading zero has to be set, too. If no further operation occurs within the next 8 seconds the SDA 2003 changes automatically to the mode of program selection. If the program-selection mode is required within the 8 s-interval, only the instruction "on" has to be set. At each setting of a new channel the controller converts this information to the corresponding frequency information which is supplied to the PLL-circuit. If there exists a corresponding station for the selected channel a picture is visible on the TV-screen.

Fig. 3.1.5



The digital tuning system incorporates also a station searching device. It is started by operating the push button for start searching "SL." In this case the controller individually supplies the frequency information, stored in the internal ROM, to the PLL-circuit. If a transmitting station is detected the search operation is automatically interrupted by the signal "search stop."

With the push buttons for fine tuning plus "FT+" and for fine tuning minus "FT-" frequency deviations from +3.875 to -4 MHz of the nominal channel frequency can be individually adjusted in steps of 125 kHz. If one of these push buttons is constantly pressed the fine tuning operates automatically within an interval of 250 ms. The above mentioned frequencies are the overflow limits. If one of these limits is reached as long as the push button is operated, the channel display blinks. For every tuned station the corresponding channel number and the fine tuning information can be stored in the tuning memory by operating the memory-key. The ROM of the controller contains a frequency information for 100 TV channels and the band selection information, which means VHF-range band I and III as well as UHF-range.

The data is transferred between SDA 2003 and tuning memory via a data bus. It consists of the lines for shiftclock $\overline{CNVM}$, enable signal EX/ $\overline{REC}$ and data IFO. The data word contains the channel number and the fine tuning information. From the former the mean value of the frequency information is generated and for the final value the fine tuning information, being individually for every frequency range, is added. This sum is supplied to the PLL-circuit.

The SDA 200-system also includes the following ICs: IR remote control transmitter SDA 2008, IR remote control receiver SDA 2007, LED-driver SDA 2004 and fading-in device SDA 2005. SDA 2007 and SDA 2008 are described in section 4.1 and 4.2, SDA 2004 is mentioned in section 5.1 and SDA 2005 in section 3.2.

Components for circuit 3.1.2

			Ordering code
1	Pre-divider	SDA 2001	Q67000-A1464
1	Transistor	BC 238	Q62702-C698
1	Diode	BA 127 d	Q60201-X127-D9
1	Ceramic capacitor	6.8 pF	B38062-A6060-C806
1	Ceramic capacitor	150 pF	B38066-J6151-G6
4	Ceramic capacitors	1 nF	B37462-J2102-S1
2	Resistors	56 Ω /1 W	B51276-A2560-G
2	Resistors	2.7 k Ω /0.5 W	B51261-Z4272-J1
1	Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1	Resistor	56 k Ω /0.5 W	B51261-Z4563-J1

Components for circuit 3.1.5

			Ordering code
2	Ceramic capacitors	8.2 pF/63 V	B38062-A6080-C206
2	Ceramic capacitors	47 pF/63 V	B38062-J6470-G6
1	Ceramic capacitor	4.7 pF/63 V	B37062-A6472-K6
1	MKT-capacitor	0.68 μ F/100 V	B32560-D1684-J
3	MKT-capacitors	1 μ F/250 V	B32563-D3105-J
1	MKT-capacitor	2.2 μ F/250 V	B32563-D3225-J
1	Resistor network	7 $\times$ 150 Ω /10%	B92442-A0151-K307
7	Resistors	150 Ω /0.5 W	B51261-Z4151-J1
3	Resistors	6.8 k Ω /0.5 W	B51261-Z4682-J1
2	Resistors	15 k Ω /0.5 W	B51261-Z4153-J1
1	Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
4	Resistors	18 k Ω /0.5 W	B51261-Z4183-J1
2	Resistors	20 k Ω /0.5 W	B51261-Z4203-J1
8	Resistors	10 k Ω /0.5 W	B51261-Z4103-J1
1	Resistor	16 k Ω /1 W	B51276-A2163-6
1	Resistor	5 k Ω /1 W	B51276-A2562-6
1	Resistor	5.6 Ω /0.5 W	B51261-Z4562-J1
1	Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1	Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
1	Resistor	6.2 k Ω /1 W	B51276-A2622-6
1	Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
1	Resistor	22 k Ω /0.5 W	B51261-Z4223-J1
4	Resistors	47 k Ω /0.5 W	B51261-Z4473-J1
2	Resistors	1 M Ω /0.5 W	B51261-Z4105-J1

3.2 Fading-in of Channel and Programnumber on TV-Screen

Fig. 3.2.1 shows a circuit using the fade-in IC SDA 2005. It is connected to the channel processor SDA 2003 and to the RGB-circuit TDA 2530. Figure display in the right above (spot 2) or right below (spot 1) corner of the TV-screen can be freely selected by external wiring. The figure height is 21 lines of a field. At both spots two figures can be displayed. The information for a pair of figures is serially supplied. The DATA-line is common for both pairs. Each figure pair, however, has an own enable input ENA and an own clock input CL. The serial information is transferred by the clock pulses. If a display spot is not to be used the inputs for enable and clock have to be connected to ground. As shown in fig. 3.2.1 the enable inputs are connected to the output EG of SDA 2003. The clock input CL1 (display right below) is connected to the clock output of the channel indicator and the clock CL2 (display right above) to the clock output of the program indicator. If both clock inputs are crossed, the display spots for channel and program are automatically interchanged. If the device is turned on the display spots are blanked. The fade-in IC has also the input TCR. If a signal with H-level is supplied to it the display is suppressed on the screen, i.e. the duration of channel or program display can be controlled. There is also no display when the enable signal has H-level. If the enable signal had temporarily an H-level with the absence of clock pulses the previous content is again displayed.

The integrated oscillator operates accordingly to the start-stop-principle. The frequency is determined by a π -section connected to pins 15 and 16. It includes a 200 μ H-coil and two 50 pF-capacitors. Due to the start-stop-principle the oscillator is synchronized in proper phase with the line frequency.

Channel and program numbers can be displayed either on a black and white or on a colour screen. According to the screen the video signal is either superimposed on the Y-signal via a coupling diode or it influences the Y-signal as well as the colour difference signal via two blanking transistors. In this case green, red or blue figures can be displayed. For mixed colours three transistors are required as two colour difference signal channels have to be controlled.

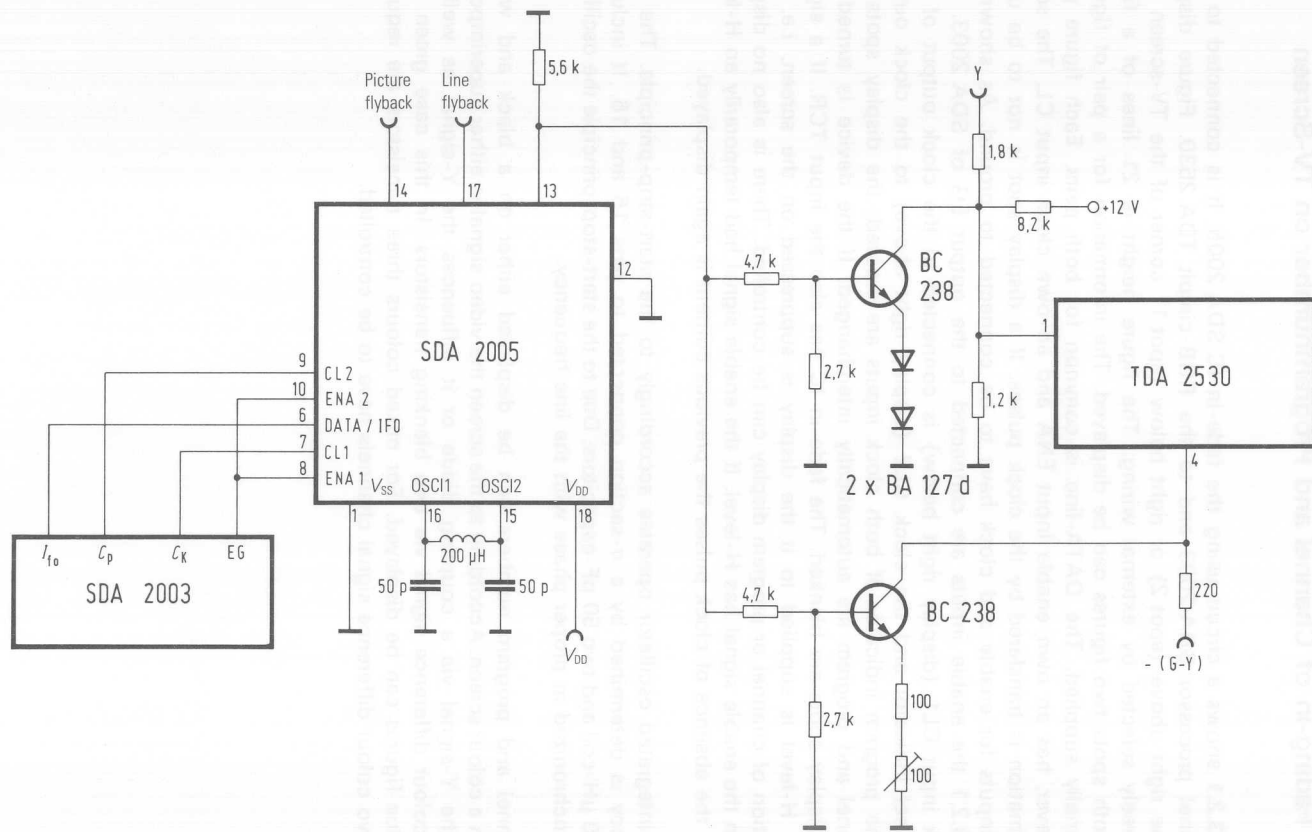


Fig. 3.2.1

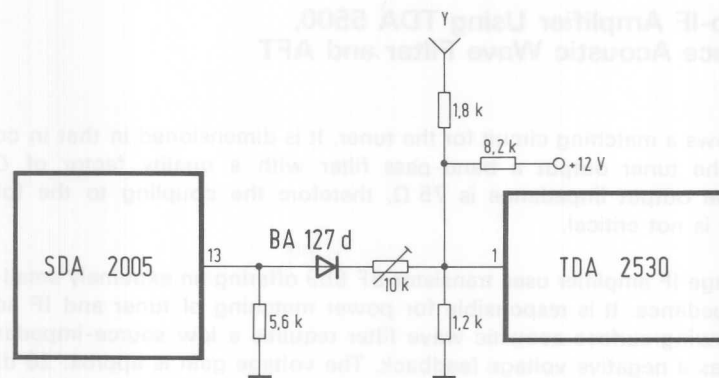


Fig. 3.2.2

Components for circuit 3.2.1

		Ordering code
1 Channel processor	SDA 2003	Q67120-C32
1 Fade-in IC	SDA 2005	Q67100-Y502
1 Video-matrix IC	TDA 2530	Q67000-A1295
2 Transistors	BC 238	Q62702-C698
2 Diodes	BA 127 d	Q60201-X127-D9
2 Ceramic capacitors	47 pF/63 V	B38062-A6470-G6
1 Resistor	100 Ω /0.5 W	B51261-Z4101-J1
1 Resistor	220 Ω /0.5 W	B51261-Z4221-J1
1 Resistor	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	1.8 k Ω /0.5 W	B51261-Z4182-J1
2 Resistors	2.7 k Ω /0.5 W	B51261-Z4272-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	5.6 k Ω /0.5 W	B51261-Z4562-J1
1 Resistor	8.2 k Ω /0.5 W	B51261-Z4822-J1
additional for circuit 3.2.2		
1 Diode	BA 127 d	Q60201-X127-D9
1 Resistor	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	1.8 k Ω /0.5 W	B51261-Z4182-J1
1 Resistor	5.6 k Ω /0.5 W	B51261-Z4562-J1
1 Resistor	8.2 k Ω /0.5 W	B51261-Z4822-J1

3.3 Video-IF Amplifier Using TDA 5500, Surface Acoustic Wave Filter and AFT

Fig. 3.3 shows a matching circuit for the tuner. It is dimensioned in that in conjunction with the tuner output a band-pass filter with a quality factor of $Q=7$ is realized. The output impedance is $75\ \Omega$, therefore the coupling to the following IF amplifier is not critical.

The one-stage IF amplifier uses transistor BF 959 offering an extremely small reverse transfer impedance. It is responsible for power matching of tuner and IF amplifier. As the following surface acoustic wave filter requires a low source-impedance the transistor has a negative voltage feedback. The voltage gain is approx. 26 dB at an emitter current of 20 mA. This compensates sufficiently the 22 dB-insertion-loss of the following surface wave filter. The dynamic range of transistor BF 959 reaches its maximum at an emitter current of 20 mA. If the delayed tuner control is correctly adjusted no cross-modulation products are generated.

The surface acoustic wave filter OFW 361 (G-standard) consisting of lithium niobat replaces a conventional compact-coil filter. Tuning as well as post-tuning because of aging effects are not necessary. Frequency characteristic and group delay are determined by the geometry of the integrated converters and correspond to actual standards.

The integrated video-IF amplifier TDA 5500 amplifies the symmetrically-applied IF signal. A keyed control keeps the video output voltage constant in a voltage range of max. 55 dB.

TDA 5500 contains also a limiting amplifier. Its outputs at pin 8 and 9 are connected to an auxiliary circuit, being tuned to a carrier frequency of 38.9 MHz.

By an additional series 12 pF-capacitor a trap for 36.15 MHz is realized and thus video interference effects are efficiently suppressed (sound rattling). The video frequency is derived from the video IF by means of a demodulator controlled at a frequency of 38.9 MHz. The positive and the negative video signals are available at pins 11 and 12 with an amplitude of $3\ V_{pp}$. The max. current of these outputs is 5 mA.

The standard output at pin 10 is provided for VCR-operation ($1\ V_{pp}$ at $75\ \Omega$). With a switching voltage of 12 V video playback is chosen instead of recording. This voltage is supplied via a diode BA 127 and a $2.7\ k\Omega$ -resistor to pin 4. It turns off the video-IF amplifier. Besides that this voltage increases via another diode and an $820\ \Omega$ -resistor the level at the emitter of transistor BF 959 as long as it becomes non-conductive. Thus an interference of any station is reliably avoided at VCR-playback.

The white level is adjusted by the potentiometer connected to pin 14. The synchronous level is always kept constant during the adjustment procedure.

The sound-IF signal is attenuated by approx. 20 dB by means of a 5.5 MHz-trap.

A current of up to 15 mA can be applied to pin 5 of the TDA 5500 for controlling the tuner. The threshold is adjustable by the potentiometer connected to pin 6.

A special IC TDA 4260 is responsible for AFT. This device limits the video carrier of 38.9 MHz, which controls the coincidence demodulator. In conjunction with the tuned circuit connected to pins 7 and 8 it operates as frequency discriminator. According to the frequency deviation at the input a negative or positive current is available at pin 5. A correcting signal is generated by a resistor network and superimposed to the tuning voltage. The control characteristic can be varied by the resistor network connected to pin 4 to meet better the different frequency deviations in the VHF- and the UHF-range. The described circuit operates advantageously with a current of 1 mA in the VHF-range and with one of 0.25 mA in the UHF-range.

The TDA 4260 is weakly coupled via two 10 pF-capacitors to the demodulator of TDA 5500. Therefore a sufficiently small and symmetrical capture range is realized. A change from one to another channel is easily guaranteed even if the AFT is turned on. The AFT is ineffective by switching off the limiting amplifier of the TDA 4260 by shifting the level at pin 3.

Fig. 3.3

Components for circuit 3.3

		Ordering code
1 Video-IF IC with VCR connection	TDA 5500	Q67000-A1377
1 AFC-IC mit programmable current deviation	TDA 4260	Q67000-A1300
1 Transistor	BF 959	Q62702-F640
2 Diodes	BA 127	Q60201-X127-D9
1 Surface acoustic wave filter	OFW 361	B39936-A1-X18
2 Ceramic capacitors	10 pF/500 V	B38116-J5100-J1
1 Ceramic capacitor	82 pF/63 V	B38066-J6820-G6
1 Ceramic capacitor	100 pF/50 V	B37979-J5101-J
1 Ceramic capacitor	680 pF/63 V	B37062-A6681-K6
4 Ceramic capacitors	1 nF/63 V	B37062-A6102-K6
3 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
5 Ceramic capacitors	100 nF/63 V	B37449-F6104-S2
1 Electrolytic capacitor	4.7 μ F/16 V	B41313-A4475-V
1 Electrolytic capacitor	22 μ F/25 V	B41313-A5226-T
1 Electrolytic capacitor	470 μ F/10 V	B41283-A4477-T
1 Resistor	47 Ω /1 W	B51276-A2470-G
1 Resistor	100 Ω /1 W	B51276-A2101-G
1 Resistor	820 Ω /0.5 W	B51261-Z4821-J1
3 Resistors	1.2 k Ω /0.5 W	B51261-Z4272-J1
1 Resistor	2.7 k Ω /0.5 W	B51261-Z4272-J1
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
2 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
1 Resistor	56 k Ω /0.5 W	B51261-Z4563-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	470 k Ω /0.5 W	B51261-Z4474-J1
1 Resistor	560 k Ω /0.5 W	B51261-Z4564-J1
1 Filter	D 10 N (Fa. Toko)	} without ordering code
1 Filter	D 10 NA (Fa. Toko)	
1 Filter	D 11 N (Fa. Toko)	
1 Choke	1.2 μ H (Fa. Salota)	
1 Choke	7.5 μ H	
2 Chokes	9 μ H	
2 Potentiometers	5 k Ω	

3.4 Video-IF Amplifier with Quasi-Parallel-Sound IC

Fig. 3.4 shows a modified video-IF circuit using the IC TDA 2840 for quasi-parallel sound operation. The generator of the composite colour signal as well as the AFT-circuit are the same as described in section 3.3. The advantage of this application is essentially in that the sound IF of 5.5 MHz is separately generated by the quasi-parallel sound IC, type TDA 2840. The sound carrier (33.4 MHz) of the video-IF-signal is not attenuated by the sound trap of the surface acoustic wave filter OFW 361 before it is demodulated, as the video-IF-signal is already picked up at the IF-prestage transistor BF 959. Therefore the signal-to-noise ratio of the quasi-parallel sound is increased by the insertion loss of the sound trap. Besides that video-interferences for the sound are reduced by an advanced 38.9 MHz-carrier generation of the quasi-parallel sound IC TDA 2840. This IC consists of a 3-stage controlled IF amplifier with a control range of 50 dB, a coincidence demodulator with carrier generation (pin 7 and 8), a low-pass filter and an impedance converter. By the latter it is possible to connect a ceramic filter for the 5.5 MHz-sound-IF directly to pin 3 without requiring additional components.

The output voltage minimum of the 5.5 MHz-FM-IF is 10 mV. Its peak values are controlled by the IC when the input voltage increases 100 μ V.

Components for circuit 3.4

		Ordering code
1 Video-IF-IC with VCR connection	TDA 5500	Q67000-A1377
1 AFC-IC with programmable current deviation	TDA 4260	Q67000-A1300
1 Quasi-parallel-sound-IC	TDA 2840	Q67000-A1268
1 Surface acoustic wave filter	OFW 361	B39936-A1-X18
1 Transistor	BF 959	Q62702-F640
2 Diodes	BA 127	Q60201-X127-D9
2 Ceramic capacitors	3.3 pF/63 V	B38062-A6030-C306
1 Ceramic capacitor	4.7 pF/63 V	B38062-A6040-C706
1 Ceramic capacitor	39 pF/63 V	B38062-A6390-G006
2 Ceramic capacitors	10 pF/500 V	B38116-J5100-J1
1 Ceramic capacitor	82 pF/63 V	B38066-J6820-G6
1 Ceramic capacitor	100 pF/50 V	B37979-J5101-J
1 Ceramic capacitor	680 pF/63 V	B37062-A6681-K6
3 Ceramic capacitors	1 nF/63 V	B37062-A6102-K6
4 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
6 Ceramic capacitors	100 nF/63 V	B37449-F6104-S2
1 Electrolytic capacitor	4.7 μ F/16 V	B41313-B4475-V
1 Electrolytic capacitor	22 μ F/25 V	B41313-A5226-T
1 Electrolytic capacitor	470 μ F/16 V	B41283-A4477-T



Components for circuit 3.4 (continued)

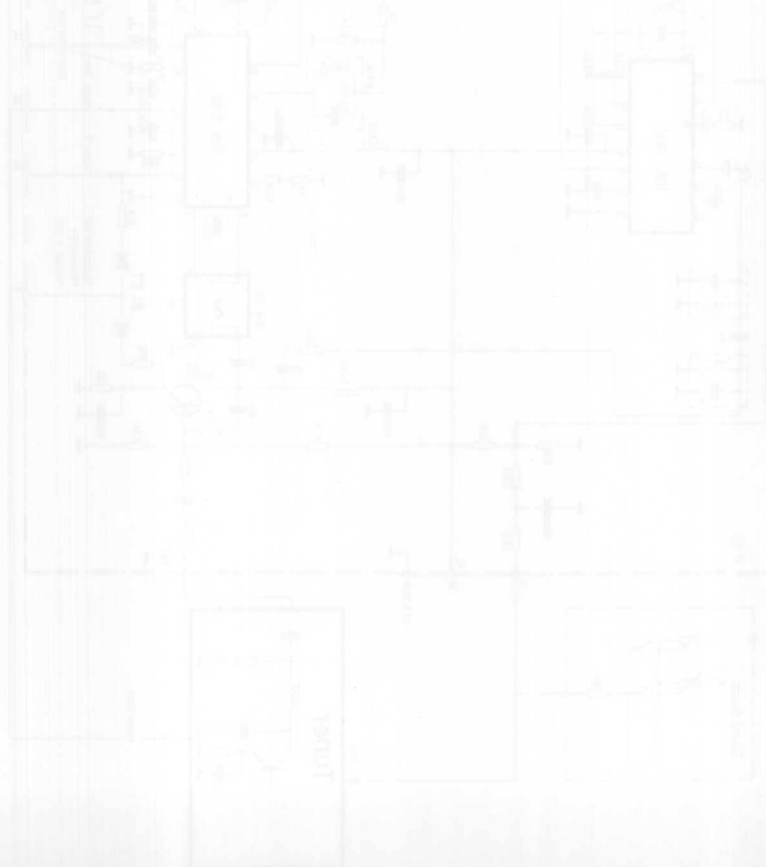
			Ordering code
1 Resistor	43 Ω /1 W		B51276-A2430-G
1 Resistor	110 Ω /1 W		B51276-A2111-G
1 Resistor	220 Ω /0.5 W		B51261-Z4221-J1
1 Resistor	820 Ω /0.5 W		B51261-Z4821-J1
2 Resistors	1.2 k Ω /0.5 W		B51261-Z4122-J1
1 Resistor	1.8 k Ω /0.5 W		B51261-Z4182-J1
1 Resistor	2.7 k Ω /0.5 W		B51261-Z4272-J1
1 Resistor	4.7 k Ω /0.5 W		B51261-Z4472-J1
1 Resistor	5.6 k Ω /0.5 W		B51261-Z4562-J1
1 Resistor	12 k Ω /0.5 W		B51261-Z4123-J1
2 Resistors	22 k Ω /0.5 W		B51261-Z4223-J1
1 Resistor	56 k Ω /0.5 W		B51261-Z4563-J1
1 Resistor	100 k Ω /0.5 W		B51261-Z4104-J1
1 Resistor	470 k Ω /0.5 W		B51261-Z4474-J1
1 Resistor	560 k Ω /0.5 W		B51261-Z4564-J1
2 Filters	D 10 N (Fa. Toko)	} without ordering code	
1 Filter	D 10 NA (Fa. Toko)		
1 Filter	D 11 N (Fa. Toko)		
1 Choke	1 μ H (Fa. Salota)		
1 Choke	7.5 μ H (Fa. Salota)		
2 Chokes	9 μ H (Fa. Salota)		
2 Potentiometers	5 k Ω		

3.5 Video-IF Amplifier with Quasi-Parallel-Sound IC and AFT

Fig. 3.5 shows a circuit with TDA 2841, which includes not only a quasi-parallel-sound circuit but also an AFT-device. The other components like preamplifier, surface acoustic wave filter, video IF-amplifier and demodulator are the same as already mentioned in section 3.3. A band-pass filter, tuned to the video-IF band is additionally connected between BF 959 and TDA 2841 to improve the far-off selectivity.

For demodulation of the sound IF (5.5 MHz) and for generating the AFT information a circuit is connected to pins 7 and 8. It is tuned to a frequency of 38.9 MHz. TDA 2841 offers also the advantage in that the current variations of the AFT-outputs correspond to the different tuning ratios. The AFT-current outputs at pins 9 and 10 are inversely poled. They can be selected with regard to desired control characteristics.

The current-deviation maximum at these outputs is ± 0.5 mA. The programming current at pin 11 can be varied in a range between 0 and 300 μ A.



Components for circuit 3.5

		Ordering code
1 Video-IF-IC with VCR connection	TDA 5500	Q67000-A1377
1 Quasi-parallel-sound IC with AFT	TDA 2841	Q67000-A1473
1 Surface acoustic wave filter	OFW 361	B39936-A1-X18
1 Transistor	BF 959	Q62702-F640
2 Diodes	BA 127	Q60201-X127-D9
2 Ceramic capacitors	3.3 pF/63 V	B38062-A6030-C306
1 Ceramic capacitor	4.7 pF/63 V	B38062-A6040-C706
1 Ceramic capacitor	100 pF/63 V	B37979-J5101-J
1 Ceramic capacitor	680 pF/63 V	B37062-A6681-K6
5 Ceramic capacitors	1 nF/63 V	B37062-A6102-K6
5 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
6 Ceramic capacitors	100 nF/63 V	B37449-F6104-S2
1 Electrolytic capacitor	4.7 μ F/16 V	B41313-A4475-V
1 Electrolytic capacitor	22 μ F/25 V	B41313-A5226-V
1 Electrolytic capacitor	470 μ F/16 V	B41283-A4477-T
1 Resistor	47 Ω /1 W	B51276-A2470-G
1 Resistor	100 Ω /1 W	B51276-A2101-G
1 Resistor	220 Ω /0.5 W	B51261-Z4221-J1
1 Resistor	820 Ω /0.5 W	B51261-Z4821-J1
2 Resistors	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	2.7 k Ω /0.5 W	B51261-Z4272-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
2 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
1 Resistor	24 k Ω /0.5 W	B51261-Z4243-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	470 k Ω /0.5 W	B51261-Z4474-J1
1 Resistor	560 k Ω /0.5 W	B51261-Z4564-J1
1 Filter	D 10 N (Fa. Toko)	} without ordering code
1 Filter	D 10 NA (Fa. Toko)	
1 Filter	D 11 N (Fa. Toko)	
1 Choke	1 μ H (Fa. Salota)	
1 Choke	7.5 μ H (Fa. Salota)	
1 Choke	9 μ H (Fa. Salota)	
2 Potentiometers	5 k Ω	

3.6 Video-IF Amplifier Using TDA 5610

Fig. 3.6 shows a circuit with TDA 5610, which incorporates not only the video-IF amplifier but also an AFT-device. If VCR-operation is required corresponding measures have to be taken. In this case the video-IF amplifier can be turned off by a VCR-switching voltage of 12 V when playback operation is desired.

The IF preamplifier and the surface acoustic wave filter are the same as described in section 3.3. The IC TDA 5610 offers the advantage in that the number of components, required externally for the IF-stage, is reduced. The TDA 5610 includes a 3-stage IF-amplifier with keyed control and with carrier-controlled demodulator. The circuit connected to pins 8 and 11 (Hartley oscillator) generates the switching carrier. It is tuned to a frequency of 38.9 MHz, which is also the resonance frequency of the AFT-circuit. The latter is connected to pins 9 and 10.

The demodulated positive and negative video signals are available at pins 13 and 14, featuring a low output impedance.

The white level is adjustable by the 5 k Ω -potentiometer connected to pin 16.

The positive video signal is supplied via a 5.5 MHz-trap to a common-emitter-circuit with BC 238. At the following divider a positive video signal of 1 V_{pp} at 75 Ω is available. Pin 12 supplies an AFT-current of max. ± 2.5 mA. It controls via a resistor network the tuning voltage of the tuner. The AFT-device is switched off, when a high resistance connection is made from pin 9 to ground.

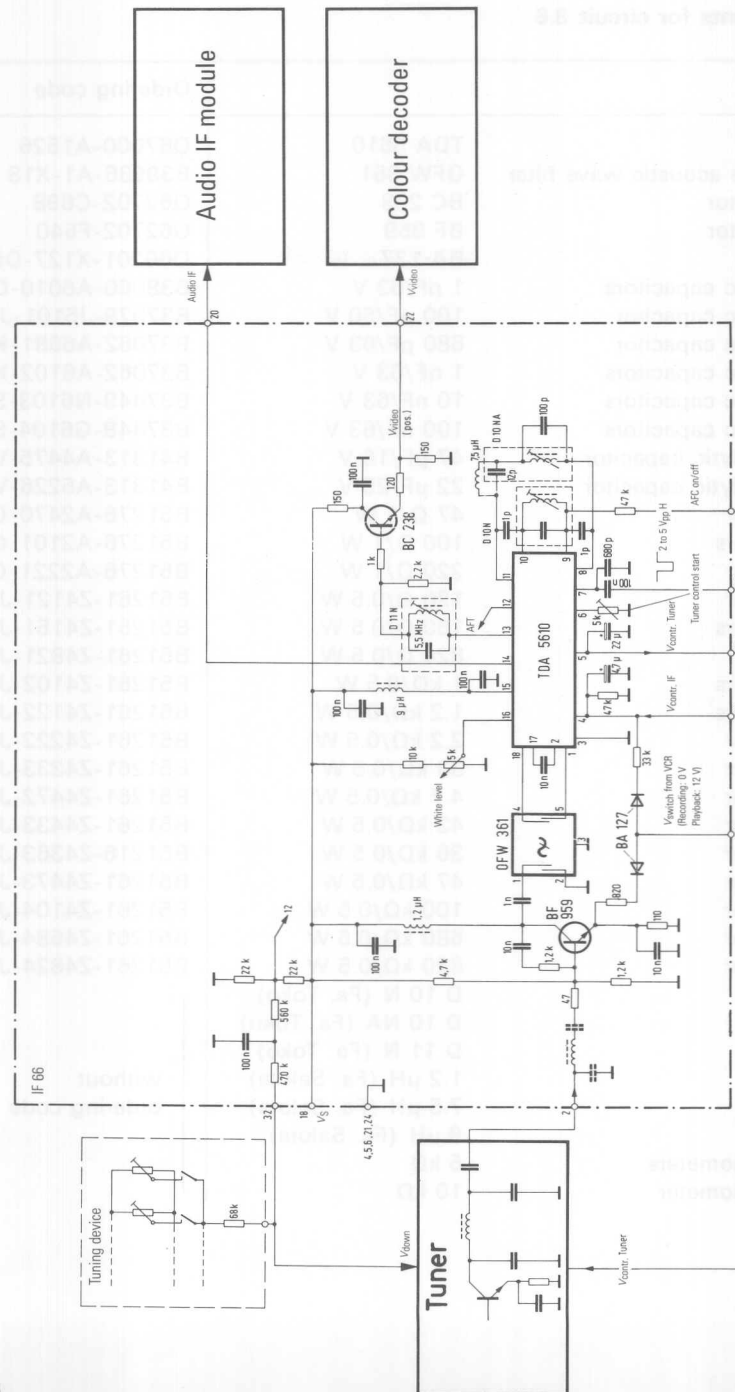


Fig. 3.6

Components for circuit 3.6

		Ordering code
1 IF-IC	TDA 5610	Q67000-A1526
1 Surface acoustic wave filter	OFW 361	B39936-A1-X18
1 Transistor	BC 238	Q62702-C698
1 Transistor	BF 959	Q62702-F640
2 Diodes	BA 127	Q60201-X127-D9
2 Ceramic capacitors	1 pF/63 V	B38060-A6010-C6
1 Ceramic capacitor	100 pF/50 V	B37979-J5101-J
1 Ceramic capacitor	680 pF/63 V	B37062-A6681-K6
2 Ceramic capacitors	1 nF/63 V	B37062-A6102-K6
3 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
6 Ceramic capacitors	100 nF/63 V	B37449-G6104-S2
1 Electrolytic capacitor	47 μ F/16 V	B41313-A4475-V
1 Electrolytic capacitor	22 μ F/25 V	B41313-A5226-V
1 Resistor	47 Ω /1 W	B51276-A2470-G
2 Resistors	100 Ω /1 W	B51276-A2101-G
1 Resistor	220 Ω /1 W	B51276-A2221-G
1 Resistor	120 Ω /0.5 W	B51261-Z4121-J1
2 Resistors	150 Ω /0.5 W	B51261-Z4151-J1
1 Resistor	820 Ω /0.5 W	B51261-Z4821-J1
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
2 Resistors	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	33 k Ω /0.5 W	B51261-Z4333-J1
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	43 k Ω /0.5 W	B51261-Z4433-J1
1 Resistor	36 k Ω /0.5 W	B51261-Z4363-J1
1 Resistor	47 k Ω /0.5 W	B51261-Z4473-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	680 k Ω /0.5 W	B51261-Z4684-J1
1 Resistor	820 k Ω /0.5 W	B51261-Z4824-J1
1 Filter	D 10 N (Fa. Toko)	} without ordering code
1 Filter	D 10 NA (Fa. Toko)	
1 Filter	D 11 N (Fa. Toko)	
1 Choke	1.2 μ H (Fa. Salota)	
1 Choke	7.5 μ H (Fa. Salota)	
1 Choke	9 μ H (Fa. Salota)	
2 Potentiometers	5 k Ω	
1 Potentiometer	10 k Ω	

The circuit shown in **fig. 3.7** includes not only the video IF-IC with AFT-device but also the quasi-parallel-sound IC TDA 4281 T. A new designed surface acoustic wave filter OFW 730 for quasi-parallel-sound application is connected to the IF preamplifier being the same as already described in section 3.3 (see fig. 3.3) OFW 730 has two symmetrical IF-outputs, one for the video IF another for the quasi-parallel-sound video-IF. Video signal and AFT-information are generated in the same way as described in section 3.6 (see fig. 3.6). As distinct from the OFW 361 the type OFW 730 has two separate paths with different frequency response and different group delay for video IF and sound IF. There is no sound trap in the video-IF path. The sound carrier of 33.4 MHz is attenuated by ≥ 40 dB. In the path for sound-IF generation, however, video carrier (38.9 MHz) and sound carrier (33.4 MHz) are processed with constant group delay. Both amplitudes are nearly the same.

The second block of function includes a multi-stage limiting amplifier which limits the output signal when the input signal is greater than 60 μV , and a coincidence demodulator. A ceramic demodulator circuit is connected to pins 14, 15 and 16. The AF signal of 300 $\text{mV}_{\text{r.m.s.}}$ being available at pin 11 is applied to a following AF amplifier. At pin 12 separate input and output are provided for VCR-recording and playback (level 600 $\text{mV}_{\text{r.m.s.}}$). The switching voltage for VCR-recording or playback operation has to be applied to pin 8.

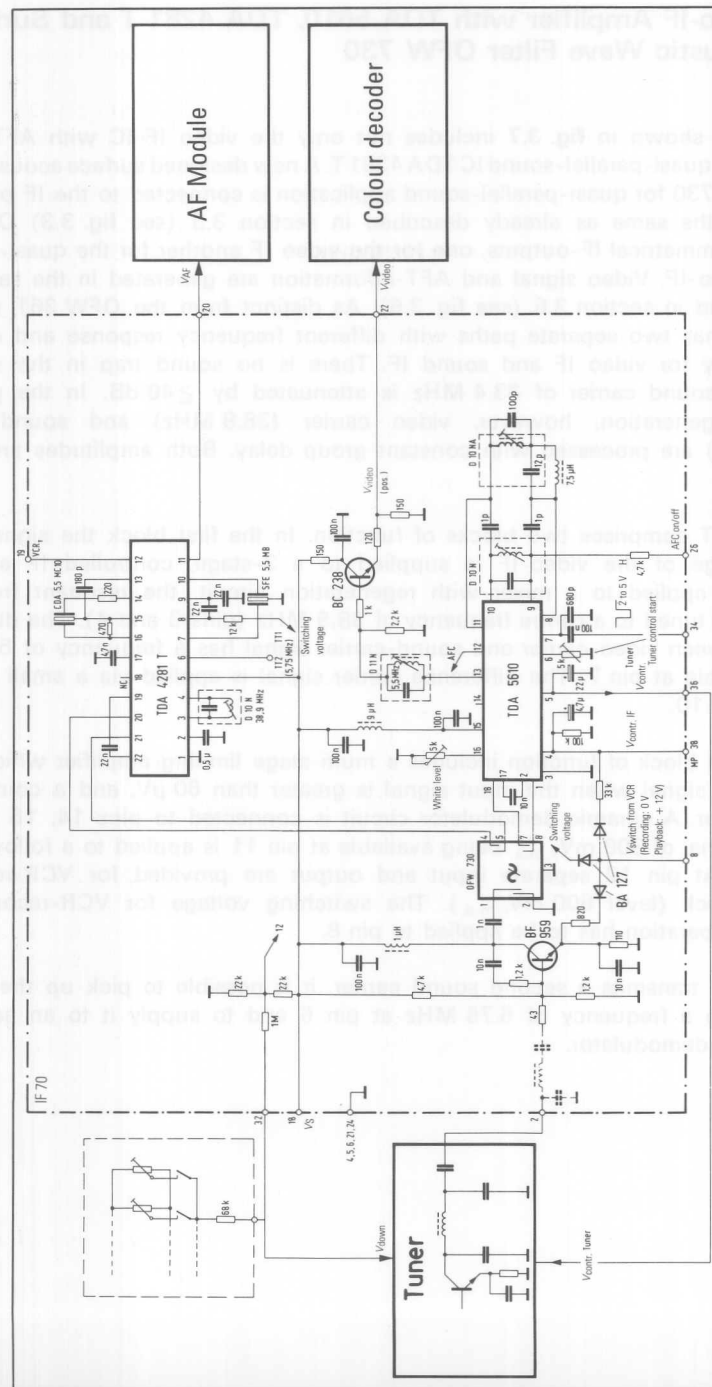


Fig. 3.7

Components for circuit 3.7

			Ordering code
1	IF-IC	TDA 5610	Q67000-A1526
1	Quasi-parallel-sound IC	TDA 4281 T	Q67000-A1589
1	Surface acoustic wave filter	OFW 730-G	B39973-A
1	Transistor	BF 959	Q62702-F640
1	Transistor	BF 238	Q62702-C698
3	Diodes	BA 127	Q60102-X127-D9
2	Ceramic capacitors	1 pF/63 V	B38062-A6010-C6
1	Ceramic capacitor	100 pF/50 V	B37979-J5101-J
1	Ceramic capacitor	680 pF/63 V	B37062-A6681-K6
1	Ceramic capacitor	180 pF/63 V	B37062-A6181-K6
1	Ceramic capacitor	1 nF/63 V	B37062-A6102-K6
1	Ceramic capacitor	4.7 nF/63 V	B37062-A6472-K6
3	Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
4	Ceramic capacitors	22 nF/63 V	B37449-F6223-S2
6	Ceramic capacitors	100 nF/63 V	B37449-F6104-S2
1	Electrolytic capacitor	4.7 μ F/16 V	B41313-A4475-V
1	Electrolytic capacitor	22 μ F/16 V	B41313-A5226-T
1	Resistor	47 Ω /1 W	B51276-A2470-G
2	Resistors	100 Ω /0.5 W	B51261-Z4101-J1
1	Resistor	120 Ω /0.5 W	B51261-Z4121-J1
2	Resistors	150 Ω /0.5 W	B51261-Z4151-J1
2	Resistors	220 Ω /0.5 W	B51261-Z4221-J1
1	Resistor	470 Ω /0.5 W	B51261-Z4471-J1
1	Resistor	820 Ω /0.5 W	B51261-Z4821-J1
1	Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
2	Resistors	1.2 k Ω /0.5 W	B51261-Z4122-J1
1	Resistor	2.2 k Ω /0.5 W	B51261-Z4222-J1
1	Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
1	Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
1	Resistor	36 k Ω /0.5 W	B51261-Z4363-J1
1	Resistor	18 k Ω /0.5 W	B51261-Z4183-J1
1	Resistor	43 k Ω /0.5 W	B51261-Z4433-J1
1	Resistor	33 k Ω /0.5 W	B51261-Z4333-J1
1	Resistor	47 k Ω /0.5 W	B51261-Z4473-J1
1	Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1	Resistor	1.5 M Ω /0.5 W	B51261-Z4155-J1
2	Filters	D 10 N (Fa. Toko)	without ordering code
1	Filter	D 10 NA (Fa. Toko)	
1	Filter	D 11 N (Fa. Toko)	
1	Ceramic filter	SFE 5.5 MB	
1	Ceramic filter	CDA 5.5 MC	
1	Choke	1.5 μ H	
1	Choke	7.5 μ H	
2	Chokes	9.1 μ H	
1	Potentiometer	5 k Ω	
1	Potentiometer	10 k Ω	

3.8 Test Pattern Generator with Frequency Synthesis

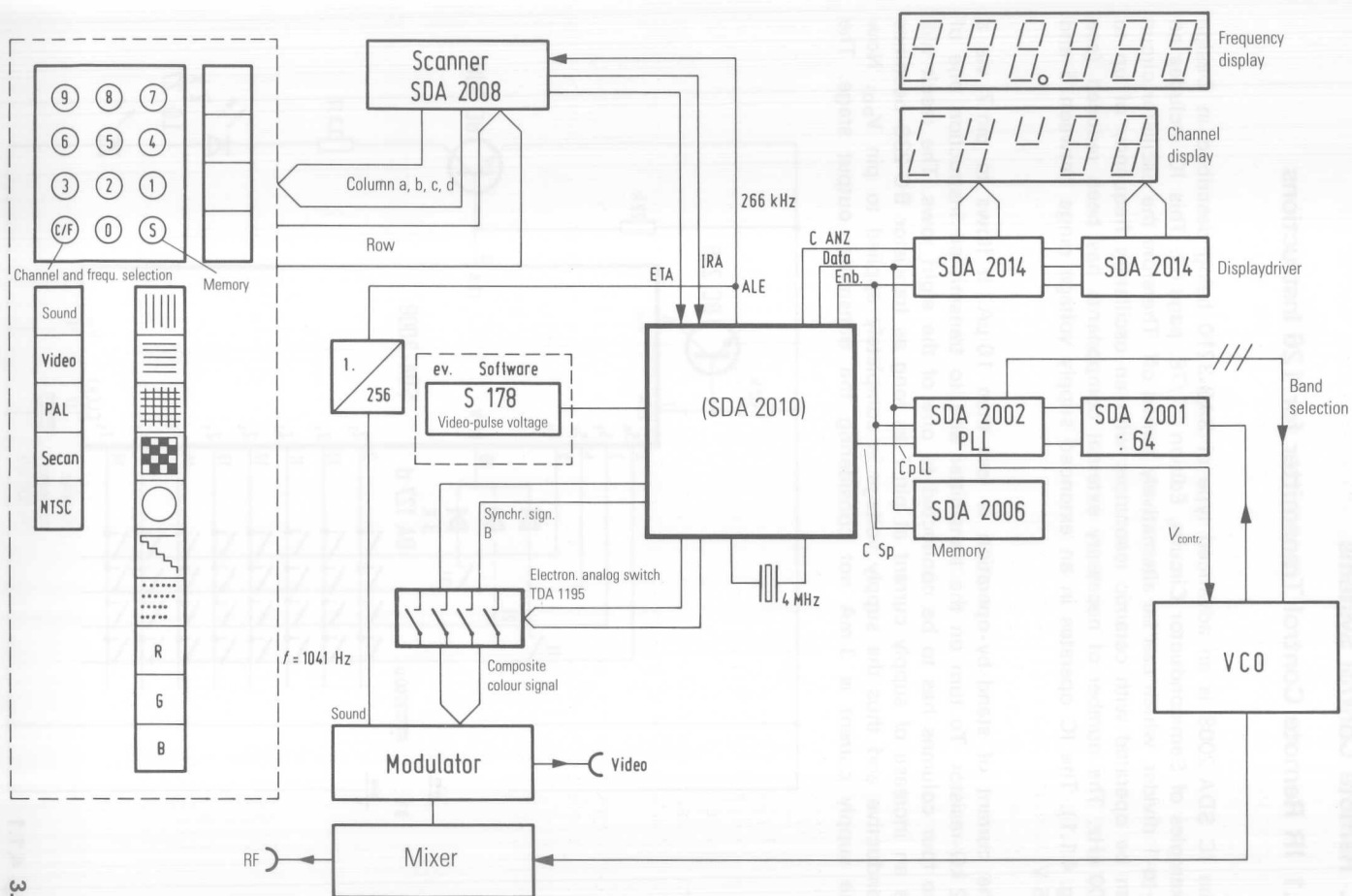
A microcomputer controlled test pattern generator can be realized by using Siemens system SDA 200 as shown in **fig. 3.8**.

The advantage of such a device for service applications is in that an accurate adjustment is possible with reference to channel patterns. Therefore TV receivers with voltage synthesis can be preset or programmed even when the device is turned off. As the searching of a TV set, operating with voltage synthesis, is not stopped when there is no carrier of a station, an accurate adjustment without generator is impossible. If conventional generators are used, only an incomplete adjustment is practicable because of their inaccurate scale. But by a test pattern generator with a program memory, which stores the local TV stations according to channel or frequency, the adjustment is essentially improved as the required information is exactly and reproducibly available at any time.

The advantages of such a concept are as follows:

- 1st An extremely accurate channel and frequency display is available.
- 2nd Special test patterns or picture series for VCR operation can be generated by software.
- 3rd Several standards are available from the generator by simple selection possibilities.
- 4th Test channels, being used very often, can be stored in a program memory.
- 5th Fading-in possibilities for channel, frequency, level and other information.

Due to these advantages the described principle is also applicable for general purpose test generators, e.g. for test devices of radio receivers, as these radio sets operate more and more in accordance to the principle of frequency synthesis or frequency counting. Besides that a very compact construction of the test device is possible.



4. Remote Control Systems

4.1 IR Remote Control Transmitter for 126 Instructions

The IC SDA 2008 is an advanced type of SAB 3210 being described in Design Examples of Semiconductor Circuits, Edition 77/78, page 63. This IC includes an 8-to-1 divider, which can be alternatively turned off. Therefore the oscillator circuit can be operated with ceramic resonators with an oscillation frequency of up to 500 kHz. The number of necessary external components has been reduced (see fig. 4.1.1). The IC operates in an extended supply voltage range between 5 and 16 V.

The current of stand-by-operation is less than $10\text{ }\mu\text{A}$. It flows to pin 7 via a $22\text{ k}\Omega$ -resistor. To turn on the transmitter and to transmit an instruction one of the four columns has to be connected to one of the eight rows. The result will be an increase of supply current at pin 7 as long as transistor BC 238 becomes conductive and thus the supply voltage is completely applied to pin V_{DD} . Now the supply current is 3 mA not considering the transmitter output stage. The

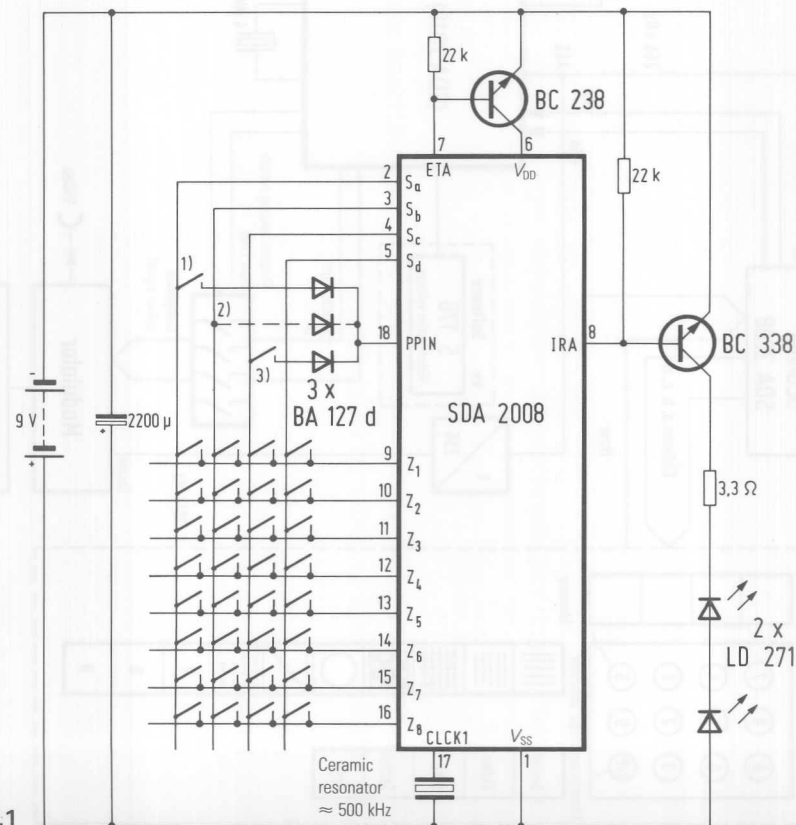


Fig. 4.1.1

SDA 2008 supplies sufficient current at output IRA that only one transistor, type BC 338, is necessary to drive directly the infrared-light-emitting diodes. The ceramic resonator as a frequency-determining component has to be connected to pin 17 and to the power supply. The reference level is applied to pin 1.

By making special connections to pin 18 the following extension can be realized:

Connection of pin 18 to:	Function:
Column a	shifting to the second instruction group
Column b	shortened distance between two instructions
Column c	start-bit="0"
Column d	no carrier for IRA-signal
IRA	by-passing of prescaler

If more than one function are required diodes have to be connected to pin 18 and to the corresponding columns as shown in fig. 4.1.1.

Instruction extension

The number of instructions can be easily extended by inserting a "shift-push-button" or by changing the start-bit. Besides that it is possible to realize a fifth matrix column as demonstrated in fig. 4.1.2. By connecting the row inputs 1 to 8 to

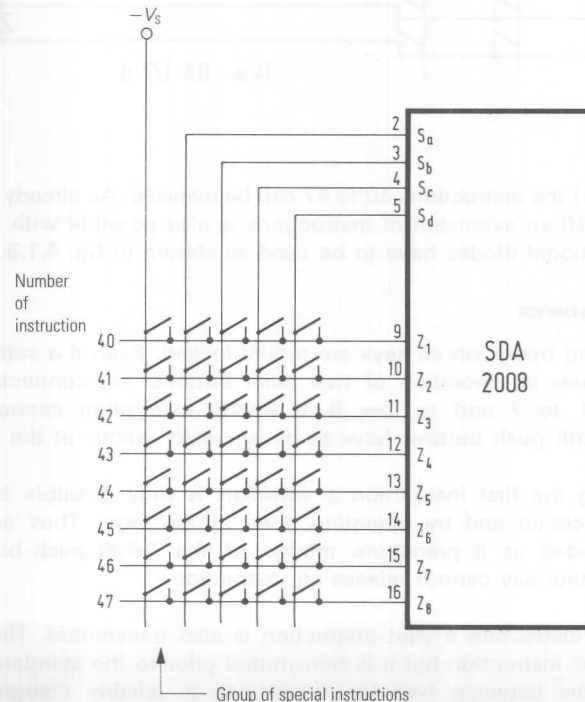


Fig. 4.1.2

Group of special instructions

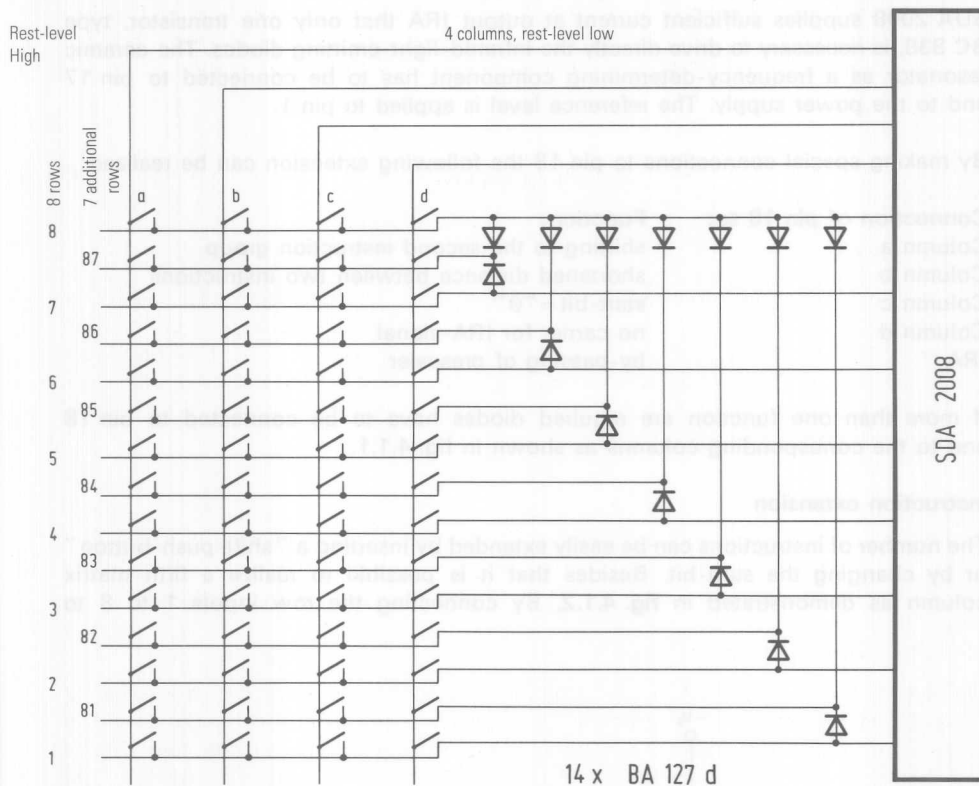


Fig. 4.1.3

V_s (power supply) the instructions 40 to 47 can be released. As already demonstrated with the SAB 3210 an extension of instructions is also possible with IC SDA 2008. In this case additional diodes have to be used as shown in **fig. 4.1.3**.

Locking measurements

In case of a wrong operation all keys are totally locked. Even if a setting of special instructions requires an operation of two push buttons, i.e. connecting a column to one of row 1 to 7 and to row 8, a wrong instruction cannot be realized as in this case both push buttons have to be operated exactly at the same time.

After transmitting the first instruction a variation is only possible by turning off the transmitting circuit and by operating none of the keys. Thus another wrong operation is avoided as a premature release of the "shift-push-button" or the operation of another key cannot release an instruction.

Besides the end-instruction a start-instruction is also transmitted. The latter corresponds to the end-instruction but it is transmitted prior to the standard instructions. Therefore the time between two key operations is reliably recognized and the

time interval for gain control of the receiver-preamplifier becomes longer. The key matrix is scanned after approx. 20 ms which are assumed for the key bounce time. By connecting pin ETA to V_{SS} this bounce time can be eliminated.

Reset

If high level is simultaneously applied to columns a and b, instruction register and program control are reset.

Biphase code

The set instruction is converted to a biphase code by the transmitter circuit. A pretrigger pulse and a start-bit, which can be selected by appropriate connection to pin PPIN, are transmitted previous to the six instruction bits. The pretrigger pulse enables a simple gain control of the receiver-preamplifier. By utilizing two different start-bits it is possible to operate two separate receivers, e.g. one of a TV-set and one of a radio, by only one remote control box.

Instruction intervals

The interval between two transmitted instructions is 12 fold of the instruction time. It can be reduced by a factor of approx. 5 by connecting column b to pin PPIN. Thus large instruction intervals are avoided at low clock frequencies.

Operation of several transmitters

Fig. 4.1.4 shows two SDA 2008 being connected in cascade. This operation is possible as program and instruction register are reset when columns a and b are synchronously set to H-level. This is attained by means of the two diodes D_1 and D_2 , which are connected to column S_a of the master transmitter. The two pins 8 (IRA) are parallel-connected. The two SDA 2008 utilize the same clock generator with ceramic resonator and both are commonly set via V_{DD} by means of transistor BC 238.

Components for circuit 4.1.1

		Ordering code
1	IR remote-control system transmitter	SDA 2008
1	Transistor	BC 238
1	Transistor	BC 338
2	IR-LEDs	LD 271
3	Silicon diodes	BA 127 d
1	Electrolytic capacitor	2200 μ F/16 V
2	Resistors	22 k Ω /0.5 W
1	Resistor	3.3 Ω /0.4 W

Component for circuit 4.1.2

1	IR remote control system transmitter	SDA 2008
		Q67100-Y503

Components for circuit 4.1.3

1	IR remote control system transmitter	SDA 2008
14	Silicon diodes	BA 127 D
		Q67100-Y503
		Q60201-X127-D9

Components for circuit 4.1.4

2	IR remote control system transmitters	SDA 2008
1	Transistor	BC 238
1	Transistor	BC 338
2	IR-LEDs	LD 271
2	Diodes	BA 127 d
1	Resistor	3.3 Ω /0.4 W
2	Resistors	22 k Ω /0.5 W
		Q67100-Y503
		Q62702-C698
		Q62702-C314
		Q62703-Q148
		Q60201-X127-D9
		B54311-Z5030-G301
		B51261-Z4223-J1



4.2 Receiver of IR-Remote Control System for 63 Instructions

The transmitted signals are received by a photodiode, processed in a preamplifier and applied to pin 17 (RSIG). Suitable preamplifiers have been described in Design Examples of Semiconductor Circuits, Edition 1978/79, Page 77. The integrated circuit SDA 2007 (see **fig. 4.2.1**) is an advanced type of SAB 3209 respectively SAB 4209. It accepts signals being processed as well in the SAB 3210 as in the SDA 2008. The SDA 2007 is especially suited for operation with a microcomputer. As it does not include any program memory a RAM-range of the microcomputer has to be defined.

The transmitted IR-signal consists of a 30 kHz-carrier being modulated in accordance to the bit-pattern with an interval of approx. 0.5 ms for each pulse train.

It is applied to pin RSIG of SDA 2007 and the instructions are available at series output (DATA). A selection between remote controlling a TV-set and a radio can be achieved by supplying an inverted start-bit to input STBT. The start-bit level corresponds to the level, which is applied to input STBT.

The series interface includes the outputs DATA, DLE and TE. The instruction is available at DATA. Outputs DLE and TE supply enable pulses, the trailing edge of which is coincident with the middle of the data bit. The signal levels at TUS₁

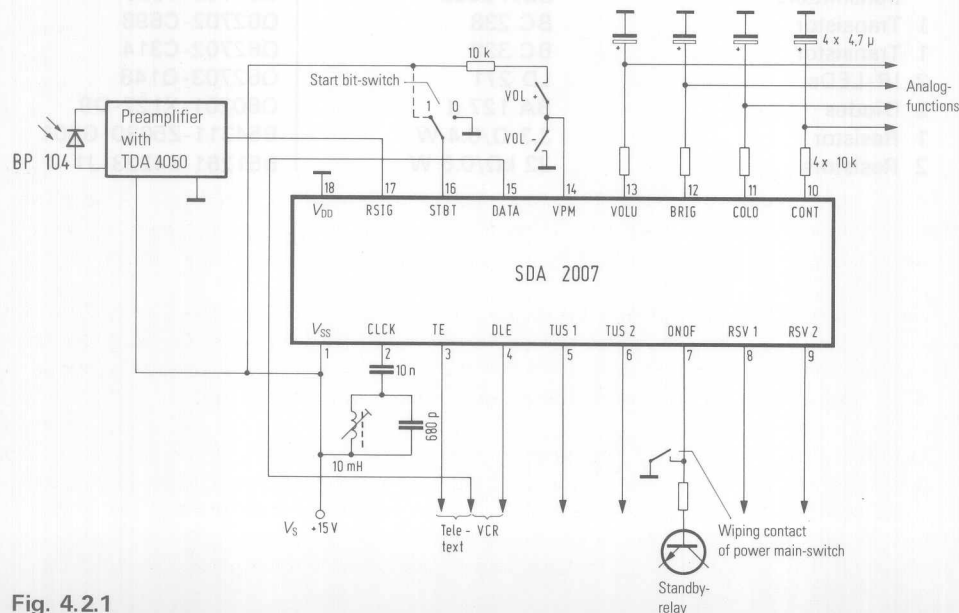


Fig. 4.2.1

	TUS 1	TUS 2	DLE-output	TE-output
TV	L	L	all instruction in repeat modus	all instructions in repeat modus
Text	H	L	DLE = L	all instructions in single modus (without end instruction) with the exception of instructions 2 and 62
Reserve	L	H		

Fig. 4.2.2

and TUS₂ are listed in **fig. 4.2.2**. These two outputs are controlled by the key selector of the remote control system.

The open-drain output stages include load resistors.

The SDA 2007 incorporates four memories for volume, brightness, colour saturation and contrast control. The analog output levels are adjustable by approx. 60 steps and square-wave voltages with a frequency of approx. 1 kHz are available at pins VOLU, BRIG, COLO and CONT. The duty cycle corresponds to the analog value. This voltage is integrated and utilized for adjustment. By instruction "standard adjustment" the analog-signal memories are set to a mask-programmed basic value. This is also realized when the supply voltage is applied to the device. The "stand-by"-state keeps all memory outputs to "low" and the last set analog values remain stored.

As long as the quick-tone flipflop is set, the memory output for volume control is kept to low level. By instruction "quick-tone" the flipflop is set to the complementary state. It is reset by instructions 16 to 25, by volume+, stand-by, standard, TUS1 or TUS2.

A manual control of volume-memory is possible by applying a signal to input VPM. Level "high" corresponds to instruction "volume+", level "low" is adequate to "volume-". The speed of changing a control value, being stored in one of the memories is approx. 8 Hz. It is the same for manual and remote control.

The power supply can be electronically switched on or off via the standby-output ONOF. A low level turns it on, a high level corresponds to stand-by. The standby-output is not only set to low level by the standby-key but also by instructions 5 to 7 and 16 to 25 and when the supply voltage is switched on.

Outputs TUS1 and TUS2 are responsible for key selection. They are driven by a flipflop each. Every push button operation at the transmitter results in changing the corresponding output of the flipflop to the complementary state.

Outputs RSV1 and RSV2 are for reserve functions. They operate in accordance to TUS1 and TUS2.

In fig. 4.2.3 a circuit with an additional SDA 2008 for manual control is shown.

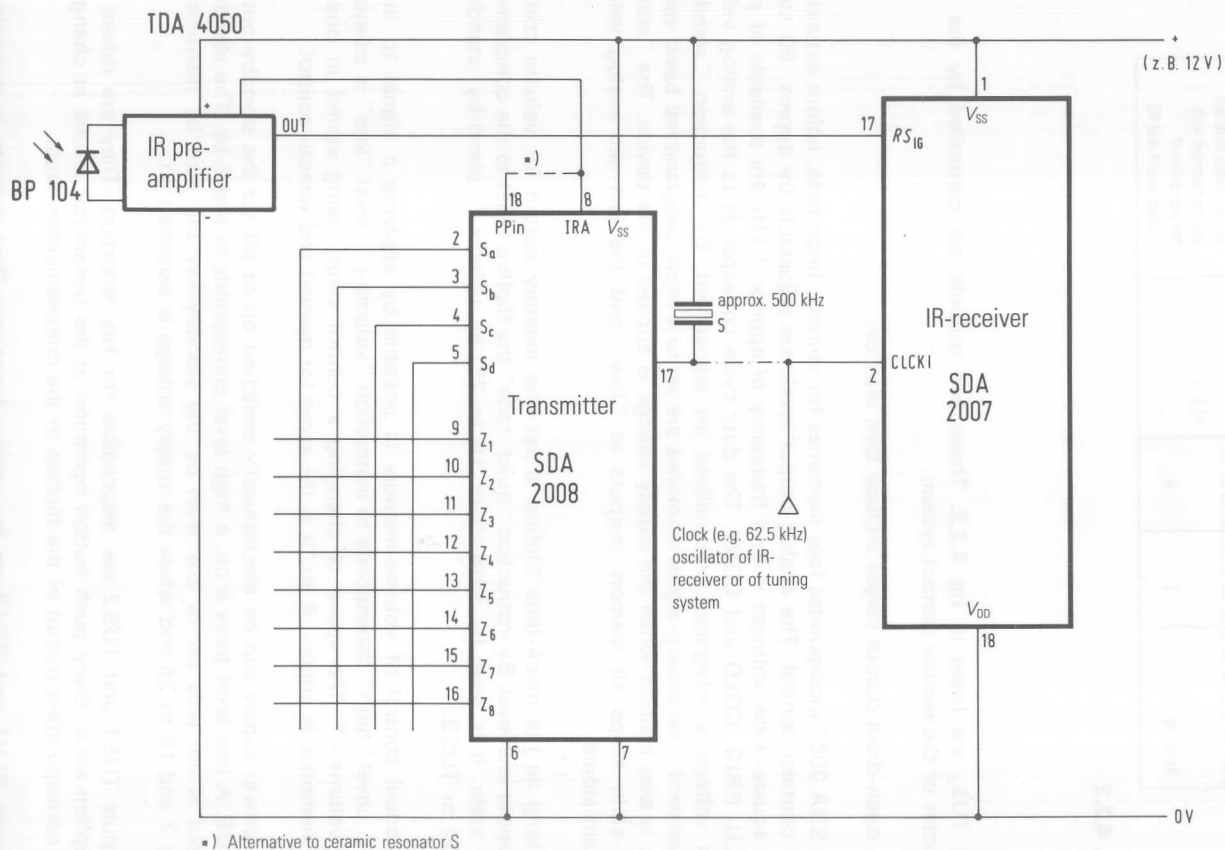


Fig. 4.2.3

Components for circuit 4.2.1

		Ordering code
1	Preamplifier	TDA 4050 B
1	IR-remote control receiver	SDA 2007
1	Photodiode	BP 104
1	Polypropylene capacitor	680 pF/160 V
1	MKH-layer capacitor	10 nF/63 V
4	Electrolytic capacitors	4.7 µF/16 V
5	Resistors	10 K/0.5 W
		B33063-B6681-H
		B32509-C103-M
		B41313-A4475-V
		B51261-Z4103-J1

Components for circuit 4.2.3

1	IR-preamplifier	TDA 4050 B	Q67000-A1373
1	IR-remote control receiver	SDA 2007	Q67100-Y504
1	IR-remote control transmitter	SDA 2008	Q67100-Y503

4.3 Digital Tuning System for Radio Sets

SDA 200 is a well-known digital tuning system for TV-sets from Siemens. A similar system for radio sets can be also realized by utilizing a frequency synthesis generator operating accordingly to the principle of phase-locked-loop. The circuit is shown in **fig. 4.3**. All operations are organized by a microcomputer, type SAB 8048. Without a fixed predivider the AM range can be tuned by 1-kHz-steps. For tuning the FM range in 25-kHz-intervals a fixed divider with a ratio of 8 to 1 and the PPL-IC SDA 2002R are required.

The frequency synthesis system incorporates the following modules: divider, PLL with range decoder, microcomputer with remote control receiver and extension circuit as well as a memory for the program. The system is provided for both remote control and manual operation. Therefore a preamplifier is also included. Frequency and operation status are displayed by several 7-segment-LEDs. Besides that the indication of the four analog functions: volume, balance, treble and bass control are realized by IC UAA 180 and LED-arrays.

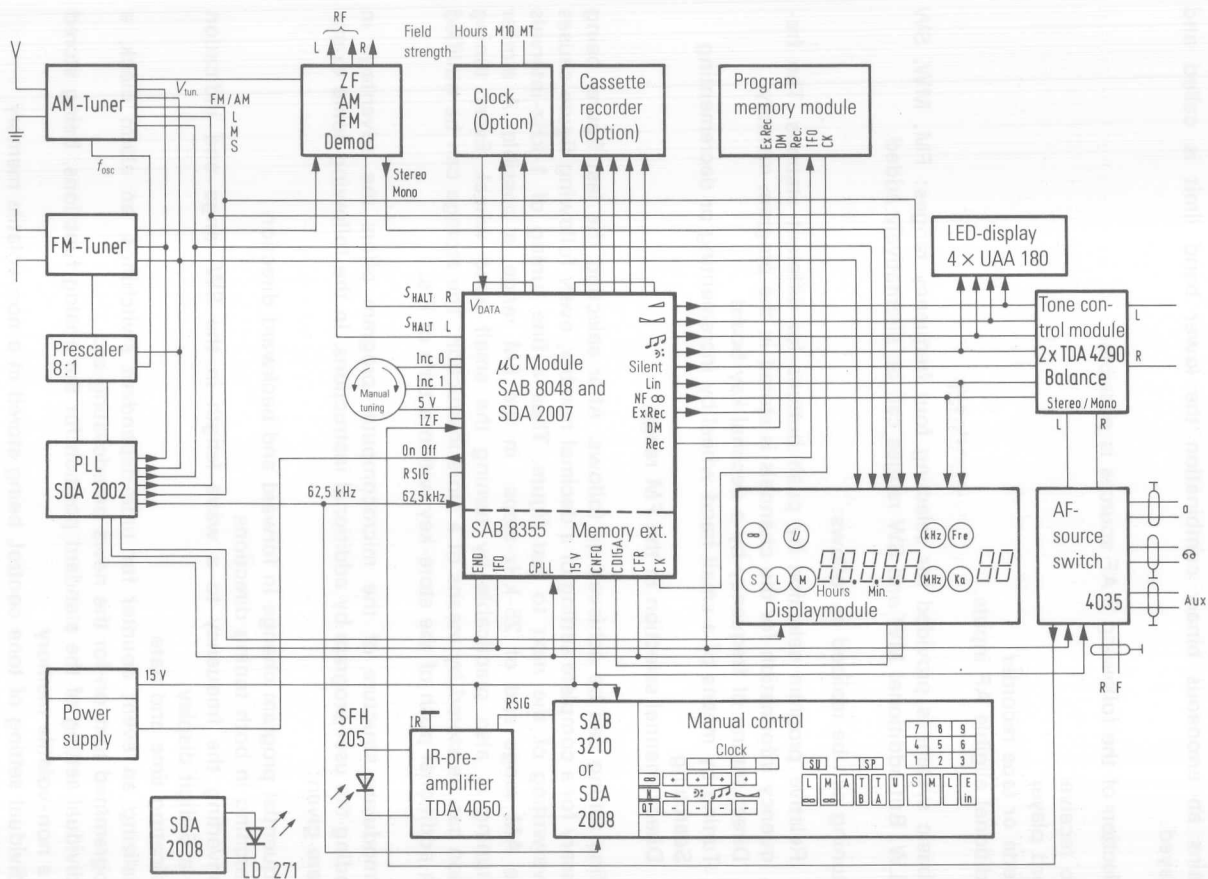
The heart of this tuning system is the single-chip microcomputer SAB 8048 being specially programmed. If a SAB 8048 is used a SAB 8355 is required for memory extension. The microcomputer realizes the following functions:

- receiving and processing of instructions being supplied from the key board or from peripheral interfaces
- receiving, decoding and processing of instructions applied from the remote control receiver SDA 2007
- controlling of data transfer to the PLL-IC SDA 2002
- controlling of data transfer to the LED display for frequency indication
- controlling of data transfer to digital addressing
- controlling of data transfer to selector of AF-sources
- controlling of bidirectional data transfer with the non-volatile program memory SDA 2006
- controlling of data transfer to channel or program indicator
- forbidden-combination-check for input data
- indicating erroneous operations by optical devices and user guidance.

Besides tuning the receiver to a transmitting station by remote control or manual operation a separate incrementing or decrementing of the binary-coded frequency information is also possible. The new tuning position can be stored by means of a special instruction. All information to and from the ICs is transferred on a common data bus. It includes the lines for data transfer IFO, for enable signals ENB and for the clock pulses. There is an additional line DM for the program memory. It is responsible for transfer of serial data.

If a mains failure occurs the system is automatically reset to stand-by operation, i.e. only IR preamplifier, IR receiver and microcomputer operate. After operating the mains switch a defined start is generated by a following start instruction and station 1 is programmed and indicated. If the memory address for the first station

Fig. 4.3



contains an erroneous binary combination the lower band limit is called and displayed.

A selection of the following 5 AF sources is possible

Radio receiver
Record player
Cassette or tape recorder
2 additional eligible AF inputs.

The basic system is provided for selecting four frequency ranges: FM, MW, SW and LW. But additional MW and SW ranges can be alternatively added.

The tuning can be realized as follows:

- 1st Relative program selection by push buttons for different stations. The frequency information for the channels is stored in the program memory
- 2nd Direct setting of frequency by a decimal key board
- 3rd Tuning by means of a small hand wheel by incrementing or decrementing
- 4th Searching
- 5th Direct channel selection in the FM range.

The fine tuning can be achieved as follows. After selecting the last figure, being necessary for a complete setting of a decimal number, every following figure causes an overwriting of the next to last figure. Thus a fine tuning of 1-kHz-intervals in the AM range and of 25-kHz-steps in the FM range is possible. A similar fine tuning is also practicable by turning the small hand wheel. Every tuning position can be stored by means of a store instruction. The storage can be nullified by an additional push of the store-key within a time of 8 s.

The modulare structure of the microcomputer program offers the advantage in extending the user program by additional instructions. In the following some examples are given:

- Sequential program change in forward and backward direction
- Searching in both tuning directions
- Converting the frequency to a wave length in the SW range and indication on a 5-digit display
- Indicating time and date
- Realizing an event counter for time-dependent switchings, an alarm clock, a programmed turn-on for the news broadcasting etc.
- Individual setting of the standard position for the analog functions, being stored in a non-volatile memory
- Individual setting of tone control, being stored in a non-volatile memory
- Searching for a stronger station
- Decoding of roadside information broadcast and range detecting
- Incremental tuning of $\pm$ functions by means of a remote control system
- Distinct user-guidance with modern displays.

The software is not described in detail, as the microcomputer IC is only supplied as a programmed device in greater quantities.

Components for circuit 4.3

			Ordering code
1	Microcomputer	SAB 8048-P	Q67120-C32-D113
1	Tuning system	SDA 2007	Q67100-Y504
1	Memory extension IC	SAB 8355 P	Q67120-R22-D88
1	IR-preamplifier	TDA 4050	Q67000-A1373
2	IR-remote control system transmitters	SDA 2008	Q67100-Y503
1	PLL-device	SDA 2002	Q67000-A1465
2	Volume and tone control ICs	TDA 4290	Q67000-A1359
1	AF source selector	4035	
4	LED-driver ICs	UAA 180	Q67000-A1104
1	Photodiode	SFH 205	Q62702-P102

4.4 Frequency Indication with SDA 5680 in SW, MW and LW-Range

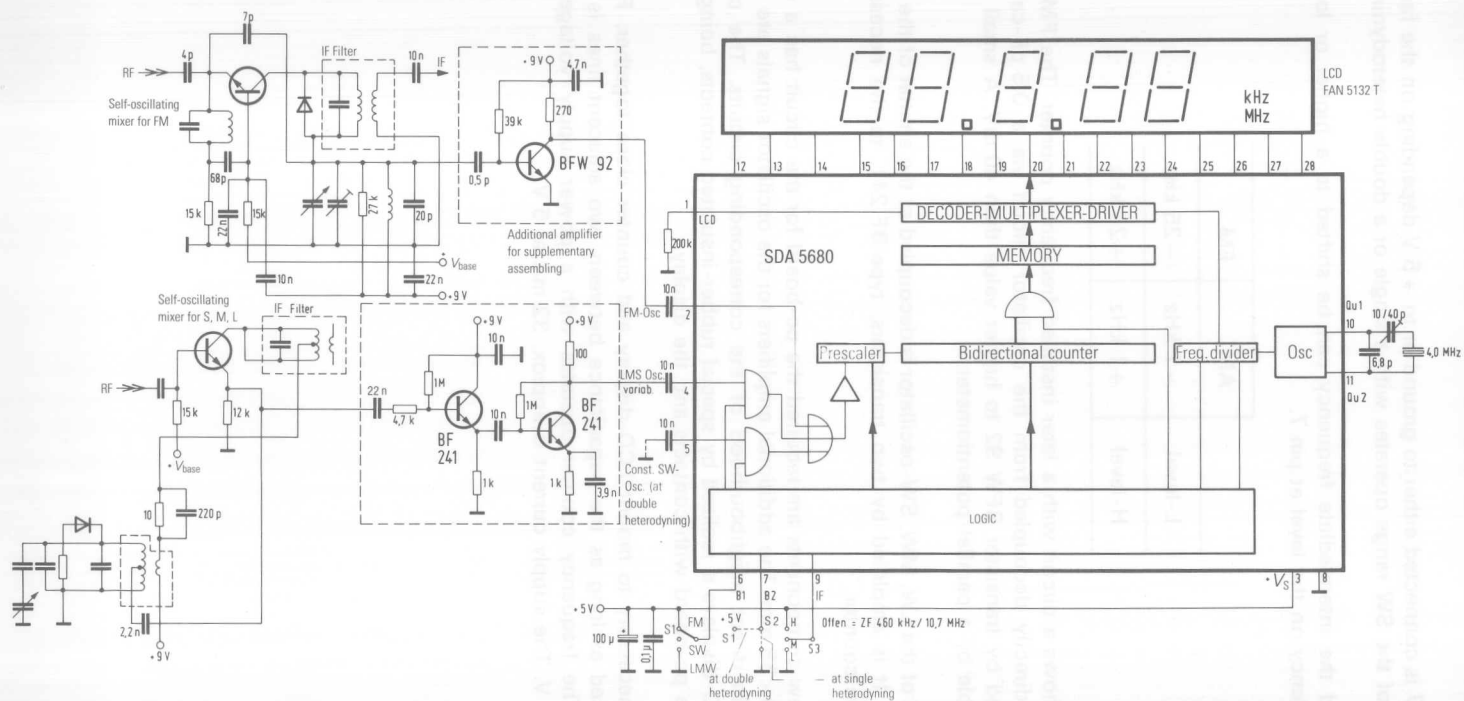
The integrated circuit SDA 5680 is a frequency counter for radio receivers. It offers the feature in that the frequency of received stations in the total SW, MW, LW and FM range is indicated. As shown in **fig. 4.4** the five-digit LCD-display FAN 5132 T is directly driven by the decoder multiplexer. If such a frequency counter is laterly installed, the required AM- and FM-signals have to be weakly decoupled from the oscillator circuit and to be amplified. Besides that the control signals, being necessary for the frequency range selection, have to be generated. New concepts, however, already consider these signal requirements. The minimum input voltages for the counter depend on the selected frequency range:

$$\begin{array}{ll} V_{i2, 4, 5} \geq 150 \text{ mV}_{\text{rms}} & 600 \text{ kHz} \leq f \leq 1 \text{ MHz} \\ \geq 80 \text{ mV}_{\text{rms}} & 1 \text{ MHz} \leq f \leq 2 \text{ MHz} \\ \geq 40 \text{ mV}_{\text{rms}} & 2 \text{ MHz} \leq f \end{array}$$

The indicated frequency of a received station is the difference between oscillator frequency and intermediate frequency. The IF is 460 kHz for the ranges SW, MW and LW and 10.7 MHz for FM. In both cases switch S_3 is in its middle position, i.e. pin 9 of the IC is open. The display assignment to the different frequency ranges is determined on the level at pin 6. This voltage is set by means of switch S_1 .

Range	Voltage level at pin 6	IF	Frequency display in
FM	$V_{i6H} \geq 2.4 \text{ V}$	10.7 MHz	MHz
SW	$0.9 \text{ V} \leq V_{i6M} \leq 1.1 \text{ V}$	460 kHz	MHz
MW/LW	$V_{i6L} \leq 0.2 \text{ V}$		kHz

Fig. 4.4



Terminal 7 is connected either to ground or to +5 V depending on the fact whether a station of the SW range operates with a single or a double heterodyning.

If required the intermediate frequency can be shifted to a higher or lower value in dependency on the level at pin 7.

	AM	FM
L-level	− 1 kHz	− 25 kHz
H-level	+ 1 kHz	+ 25 kHz

Fig. 4.4 shows a circuit with a later installed frequency counter. The FM-oscillator signal is directly decoupled from the oscillator circuit via a 0.5 pF-capacitor. It is amplified by transistor BFW 92 to higher value than 40 mV. A small mistuning is adjustable by a parallel-potentiometer.

The signal of the LW, MW, SW-oscillator is decoupled at the emitter of the frequency converter. It is amplified by two transistors, type BF 241, to the necessary input level of the counter.

As only few components are required the pc-board for the circuit has a dimension of only 50 × 55 mm. The additional amplifiers for the oscillator signals are practically mounted in direct neighbourhood of the corresponding circuits. The connection to the LCD-displays is realized by special rubber-insulated contacts, being disposed between a pc-board with contacts and the display.

It is not necessary to mount LCD-display and counter close together. Flat cables can be used as long as the capacitance between two adjacent lines is less than 500 pF. The frequency counter operates with a power supply voltage between 4.7 and 6 V. The supply current is approx. 32 mA at 5 V.

Components for circuit 4.4

		Ordering code
1 Frequency counter IC	SDA 5680 A	Q67000-Y505-A
1 LCD-display	FAN 5132 T	Q28-X658
1 Ceramic capacitor	6.8 pF/63 V	B38062-A6060-C806
1 Ceramic capacitor	2.2 pF/63 V	B37062-A6222-K6
3 Ceramic capacitors	10 nF/63 V	B37449-F6103-S2
1 Ceramic capacitor	100 nF/63 V	B37449-F6104-S2
1 Electrolytic capacitor	100 μ F/10 V	B41283-B3107-T
1 Disc trimmer	6/22 pF	—
1 Crystal	4 MHz	—
1 Socket connector	17-poles	1-163683-6 ¹⁾
1 Plug connector	17-poles	1-163749-6 ¹⁾
1 Plug connector case	9-poles	MKS5839-6-0-909 ²⁾
1 Rubber-insulated contacts	LZ 302	Q29-X111
Preamplifier for LMS-range		
2 Transistors	BF 241	Q62702-F303
1 Polypropylene capacitor	3.9 nF/160 V	B33063-B1392-H
2 Ceramic capacitors	10 nF/63 V	B37448-N6103-S2
1 Ceramic capacitor	22 nF/63 V	B37448-F6223-S2
1 Resistor	100 Ω /0.5 W	B51261-Z4101-J1
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
2 Resistors	1 M Ω /0.5 W	B51261-Z4105-J1
Preamplifier for FM-range		
1 Transistor	BFW 92	Q62702-F321
1 Ceramic capacitor	0.5 pF/500 V	B38182-A5000-B502
1 Ceramic capacitor	4.7 nF/63 V	B37062-A6472-K6
1 Resistor	270 Ω /0.5 W	B51261-Z4271-J1
1 Resistor	39 k Ω /0.5 W	B51261-Z4393-J1

¹⁾ Fa. AMP-Deutschland; 607 Langen/FFM

²⁾ Fa. STOCKO; 5600 Wuppertal 1

4.5 Receiver of Remote Control System for 5 Functions

A system for remote control of 5 functions can be realized by utilizing the IC SDA 3205. The two functions +PROG and –PROG select 16 different programs. The functions +analog and –analog can be used for volume control. The fifth function can be “on/off”. In the case of “off” the device is set to stand-by (see **fig. 4.5.1**) and output PC has high level. Therefore the program selector of the manual control is ineffective. The remote control offers the feature of changing from “stand-by” to “on” when instructions for program-selection P+ or P– are released. Usually this is not achieved with a manual control system. But with the circuit shown in **fig. 4.5.2** the same behaviour for remote and manual control can be attained. When the push button TA₁ is operated the transistor BC 238 is conductive and stand-by-output E/A (pin 11) is set to L-level. This L-level is stored in the IC SDA 3205 due to the special characteristics of its I/O-port. As the SB-output is now set to “low” (corresponds to “on”) the positive signal supplied to input PC is utilized as program selection signal P+ for the program counter. This positive voltage is separated by diode BA 127 D from the base of transistor BC 238 during stand-by state.

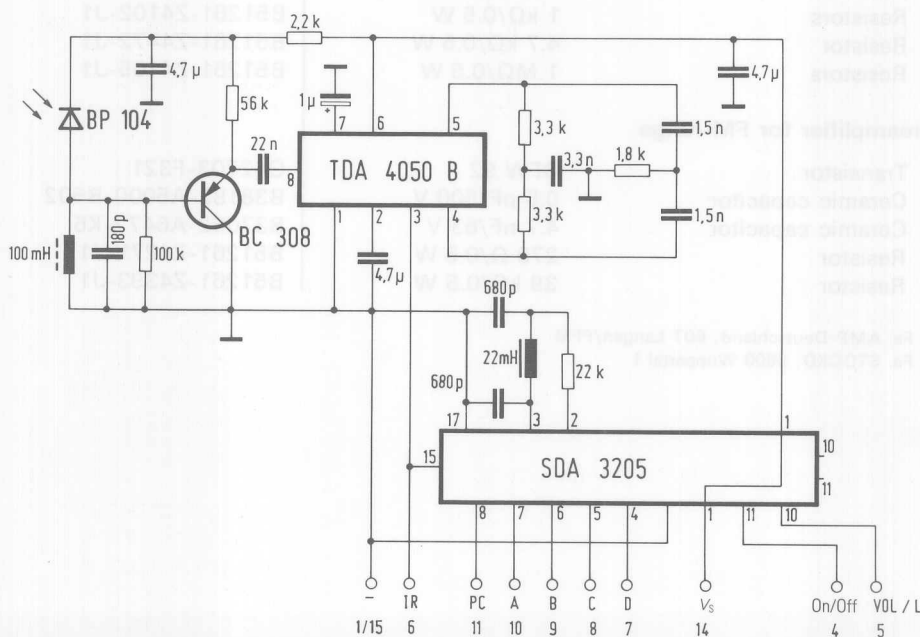


Fig. 4.5.1

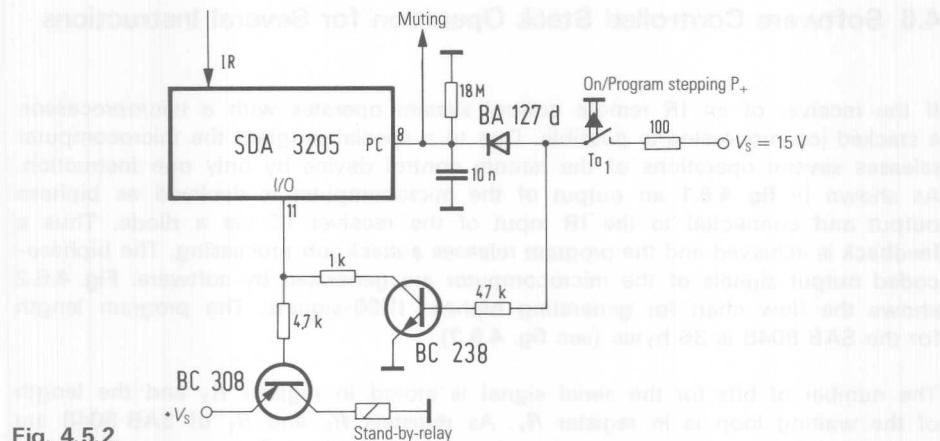


Fig. 4.5.2

Components for circuit 4.5

			Ordering code
1 IC	SDA 3205		Q67100-Y578
1 IC	TDA 4050 B		Q67000-A1373
1 Transistor	BC 416 C		Q62702-C378-V3
1 IR-Diode	BP 104		Q62702-P84
1 Coil	100 mH/screened		Fa. Salota
1 Coil	22 mH		Fa. Componex A2788
1 Styroflex capacitor	180 pF		B33063-B1181-H
2 Styroflex capacitors	680 pF		B33063-B1681-H
2 Styroflex capacitors	1.5 nF		B33063-B1152-H
1 Styroflex capacitor	3.3 nF		B33063-B1332-H
1 Ceramic capacitor	22 nF		B37448-N6223-S2
3 Tantalum capacitors	4.7 μF		B41313-A7105-V
1 Tantalum capacitor	1 μF		B41313-A7475-T
1 Resistor	1.8 kΩ		B51261-Z4182-J1
1 Resistor	2.2 kΩ		B51261-Z4222-J1
2 Resistors	3.3 kΩ		B51261-Z4332-J1
1 Resistor	4.7 kΩ		B51261-Z4472-J1
1 Resistor	22 kΩ		B51261-Z4223-J1
1 Resistor	56 kΩ		B51261-Z4563-J1
1 Resistor	100 kΩ		B51261-Z4104-J1

Additional components for immediate turn-on:

1 Transistor	BC 238 B	Q62702-C279
1 Diode	BA 127 D	Q60201-X127-D9
1 Ceramic capacitor	10 nF	B37448-N6103-S2
1 Resistor	100 Ω	B51261-Z4101-J1
1 Resistor	1 kΩ	B51261-Z4102-J1
1 Resistor	47 kΩ	B51261-Z4473-J1
1 Resistor	18 MΩ	B51264-Z4186-J1

4.6 Software Controlled Stack Operation for Several Instructions

If the receiver of an IR remote control system operates with a microprocessor, a stacked job processing is possible. Due to a special program the microcomputer releases several operations of the remote control device by only one instruction. As shown in **fig. 4.6.1** an output of the microcomputer is declared as biphasic output and connected to the IR input of the receiver IC via a diode. Thus a feedback is achieved and the program releases a stack job processing. The biphasic-coded output signals of the microcomputer are generated by software. **Fig. 4.6.2** shows the flow chart for generating biphasic IR60-signals. The program length for the SAB 8048 is 36 bytes (see **fig. 4.6.3**).

The number of bits for the serial signal is stored in register R_X and the length of the waiting loop is in register R_Y . As registers R_0 and R_1 of SAB 8048 are utilized for indirect addressing and as in this case register R_7 serves as temporary memory for the accumulator, registers R_3 to R_6 can be used for R_X and R_Y .

The total program is written as a subroutine. Before it is called the desired information has to be loaded to the accumulator.

A typical application for the described circuit is setting the bit-parallel outputs of SAB 3209 or SAB 4209 to H-level by instruction 15. This measure is necessary if the microprocessor inputs are used for data transmission as well as for key scanning.

Another application example is setting the analog functions always to normal position when another station is chosen.

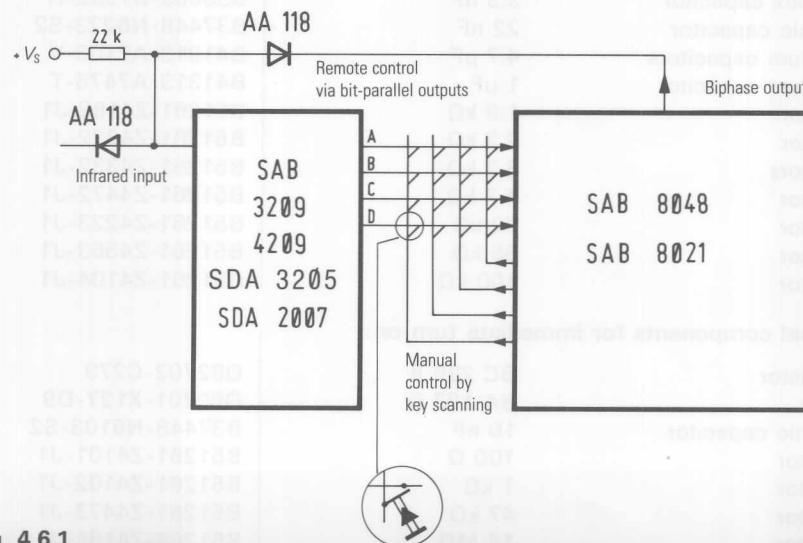


Fig. 4.6.1

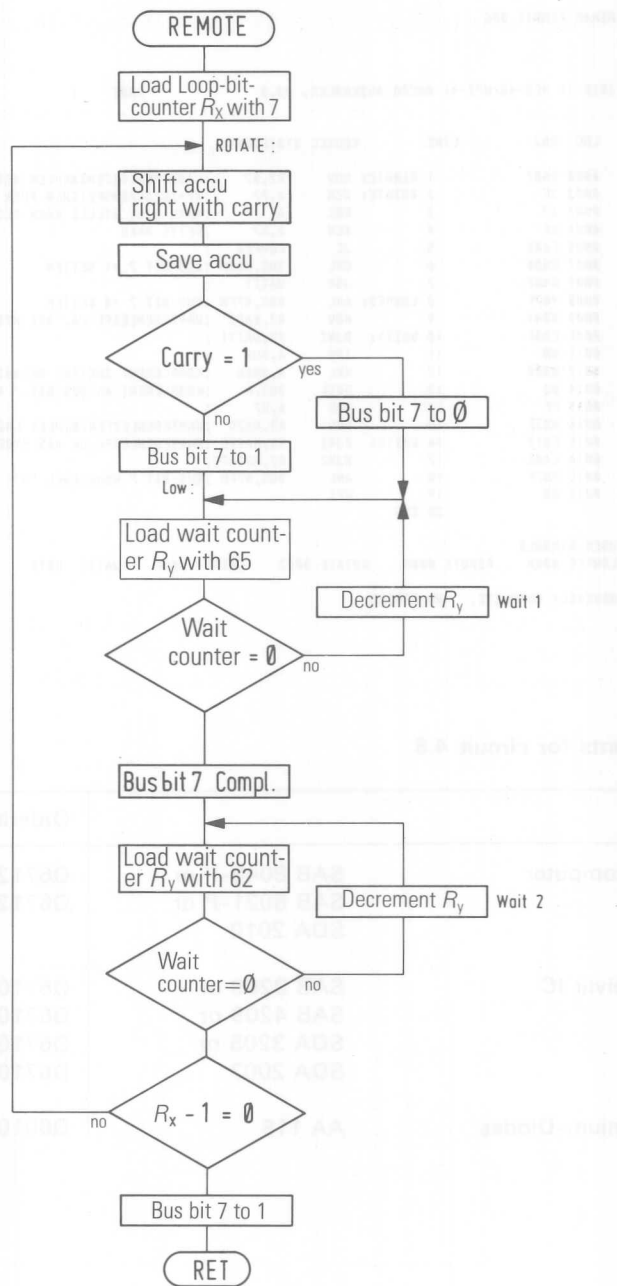


Fig. 4.6.2

LOC	OBJ	LINE	SOURCE STATEMENT
0000	BA07	1	REMOTE: MOV R2,#7 ;LADE SCHLEIFENZAehler MIT ANZAHL DER BITS
0002	2F	2	ROTATE: XCH A,R7 ;R7=ZWISCHENSPEICHER FUR AKKU
0003	67	3	RRC A ;AKKU EINE STELLE NACH RECHTS DURCH CARRY
0004	2F	4	XCH A,R7 ;RETTE AKKU
0005	F60B	5	LOWPEG ;
0007	8800	6	ORL BUS,#80H ;BUS-BIT 7 =1 SETZEN
0009	040F	7	JMP WAIT1 ;
000B	987F	8	LOWPEG: ANL BUS,#7FH ;BUS-BIT 7 =0 SETZEN
000D	BB41	9	MOV R3,#65D ;WARTESCHLEIFE CA. 488 MYSEC
000F	EB0F	10	WAIT1: DJNZ R3,WAIT1 ;
0011	08	11	INS A,BUS ;
0012	D300	12	XRL A,#80H ;KOMPLEMENT ZWEITES HALBBIT DES BIPHASE
0014	02	13	OUTL BUS,A ;KOMPLEMENT AM BUS-BIT 7 AUSGEBEN
0015	FF	14	MOV A,R7 ;
0016	8B3E	15	MOV R3,#62D ;WARTESCHLEIFENZAehler LADEN
0018	EB18	16	WAIT2: DJNZ R3,WAIT2 ;WARTESCHLEIFE CA 465 MYSEC
001A	EA02	17	DJNZ R2,ROTATE;
001C	987F	18	ANL BUS,#7FH ;BUS-BIT 7 RUHEPEGEL "H"
001E	83	19	RET
		20	END

USER SYMBOLS

LOWPEG 000B REMOTE 0000 ROTATE 0002 WAIT1 000F WAIT2 0018

ASSEMBLY COMPLETE, NO ERRORS

Components for circuit 4.6

		Ordering code
1 Microcomputer	SAB 8048-P or SAB 8021-P or SDA 2010	Q67120-C32-D113 Q67120-C64-D88
1 IR receiver IC	SAB 3209 or SAB 4209 or SDA 3205 or SDA 2007	Q67100-Y395 Q67100-Y460 Q67100-Y578 Q67100-Y504
2 Germanium-Diodes	AA 118	Q60101-X118

4.7 SDA 2008 Keyboard Input IC for Microcomputers

SDA 2008 had originally been designed for IR remote control systems. It includes a matrix scanner for a key board and a serial interface. The serial binary-coded information can be processed in a microcomputer by a simple program. The advantage of the circuit shown in **fig. 4.7.1** is in that only three connections to the microcomputer are required. The clock of SDA 2008 is directly derived from the ALE-pulses of SAB 8748. Thus the described circuit operates independently of the clock used for the microcomputer. The ETA-signal is supplied to pin P_{12} and the IRA-signal to pin P_{13} of SAB 8748.

The flow charts for serial input of the biphas information to the microcomputer are shown in **fig. 4.7.2a and b**. It is assumed that the SDA 2008 is clocked by the ALE-signal of SAB 8748. Therefore the flow chart is independent of any microcomputer clock frequency. **Fig. 4.7.3** shows the timing chart of the biphas-coded information. The dependency of the output signals ETA and IRA on the ALE-clock is shown in **fig. 4.7.4**. For better understanding an example is given, i.e. the time dependence of instruction 77 on 64 ALE-pulses each is demonstrated. **Fig. 4.7.5** shows the output signal of SDA 2008 and the microcomputer signal.

Up to 126 instructions can be processed by the described circuit with a speed of up to 25 lines/s, i.e. almost the total 7-bit-ASCII-code. The listing of subroutines SCAN, IN7BIT and UPWAIT is shown in **fig. 4.7.6**.

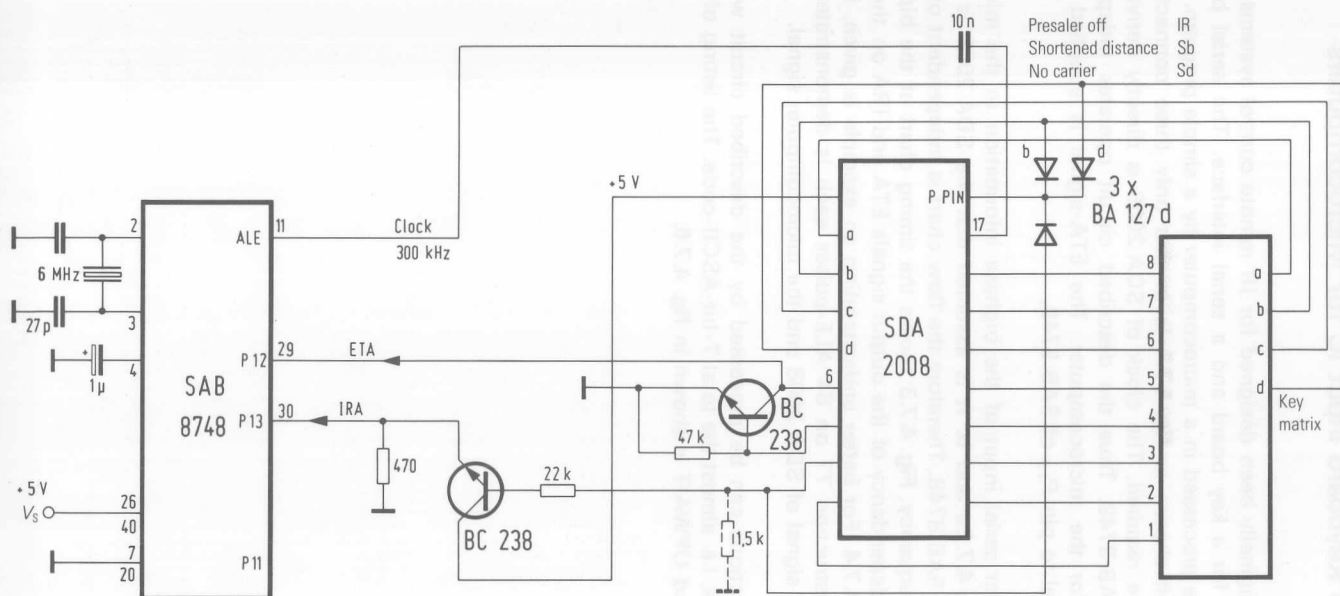


Fig. 4.7.1

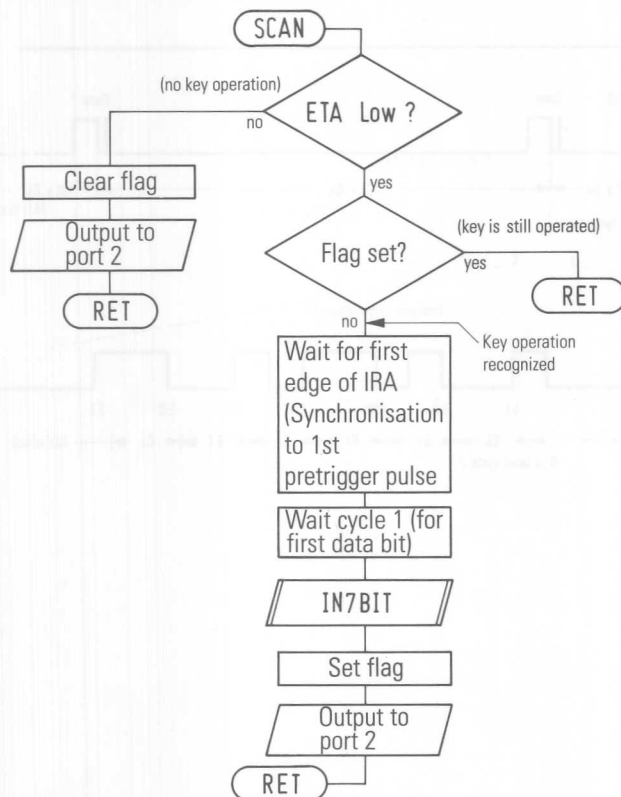


Fig. 4.7.2a

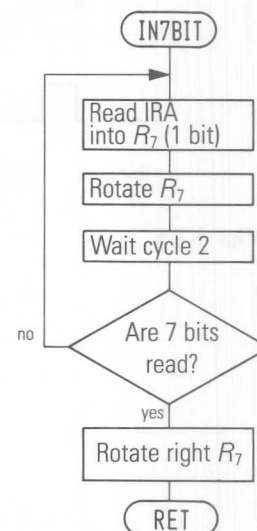


Fig. 4.7.2b

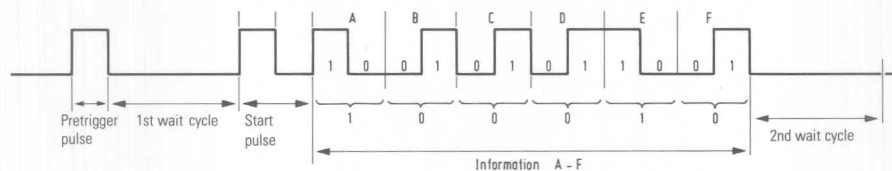


Fig. 4.7.3

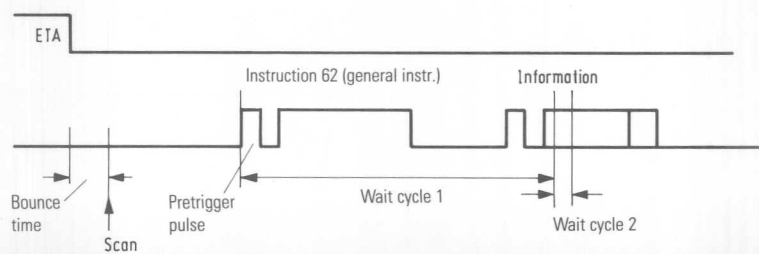


Fig. 4.7.4

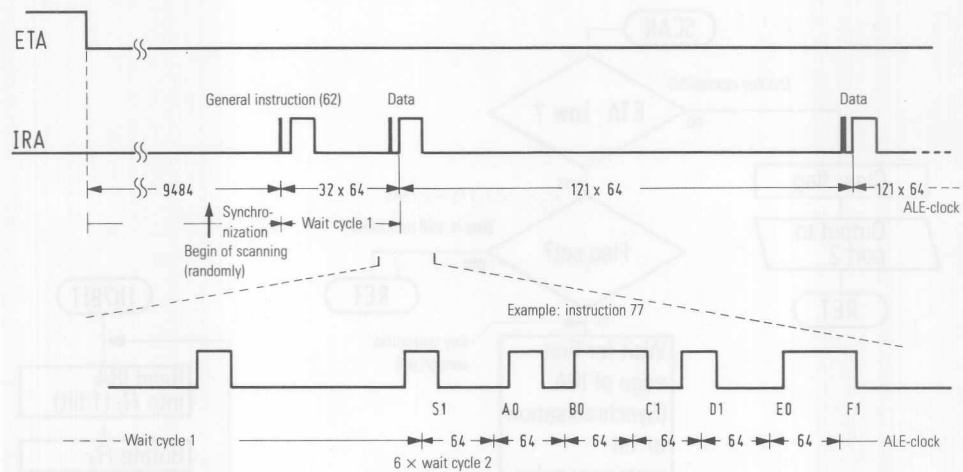


Fig. 4.7.5

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	***** PROGRAMM S C A N *****
		2	;
		3	;
		4	;
		5	DAS PROGRAMM DIENT ZUM EINLESEN DES BIPHASE-CODES
		6	EINES ANGESCHLOSSENEN SDA2000-SENDERBAUSTEINES. DER
		7	SDA2000 WIRD DABEI VOM ALE DES PROZESSORS GETAKTET.
		8	;
		9	DAS PROGRAMM IST ALS SUBROUTINE ABGEFASST UND MUSS
		10	MINDESTENS ALLE 9000 ALE-ZYKLEN EINMAL AUFGERUFEN
		11	WERDEN. DIE EINGELESENE INFORMATION WIRD HIER ALS
		12	BEISPIEL AN PORT2 BINAER AUSGEGEBEN.
		13	;;FESTLEGUNG VON KONSTANTEN:
0002		14	ETA SET 2 ; ETA LIEGT AN BIT2 / PORT1
0003		15	IRA SET 3 ; IRA LIEGT AN BIT3 / PORT1
		16	;
		17	;
		18	;
0000 00		19	ARBEIT: NOP ;HIER STEHT DAS
0001 00		20	NOP ;ARBEITSPROGRAMM
0002 00		21	NOP ;
		22	;
		23	;
		24	MODUL ZUR ABFRAGE VON ETA. SOLANGE ETA=1 IST,WIRD NICHTS UNTERNOMMEN
0003 140C		25	CALL SCAN ;
		26	;
		27	;
0005 0400		28	JMP ARBEIT ;
		29	;
		30	;
		31	*****
		32	;
		33	SUBROUTINEN
		34	;
0007 E807		35	UPWAIT: DJNZ R0,UPWAIT ;
0009 E907		36	DJNZ R1,UPWAIT ;
000B 83		37	RET ;
		38	;
		39	;;
000C 09		40	SCAN: IN A,P1 ;
000D 5304		41	ANL A,#1 SHL ETA ;
000F C617		42	JZ TASTE ; WENN ETA=0, DANN TASTE GEDRUECKT
0011 FF		43	MOV A,R7 ;
0012 537F		44	ANL A,#7FH ;LOESCHE FLAG
0014 AF		45	MOV R7,A ;
0015 3A		46	OUTL P2,A ;
0016 83		47	HALTEN: RET ;
		48	;
0017 FF		49	TASTE: MOV A,R7 ;
0018 F216		50	JB7 HALTEN ;WENN FLAG GESETZT, DANN BEF. SCHON GELESEN
		51	;
		52	WARTEN AUF ERSTEN VORIMPULS:

Fig. 4.7.6

LOC	OBJ	SEQ	SOURCE STATEMENT
001A	09	53	WAIT: IN A,P1 ;
001B	5308	54	ANL A,#1 SHL IRA ;
001D	C61A	55	JZ WAIT ;
		56	;VORIMPULS ANGEKOMMEN !! WARTEN AUF ERSTES DATEN-BIT:
001F	B858	57	MOV R0,#58H ;
0021	B905	58	MOV R1,#5 ;
0023	1407	59	CALL UPWAIT ;
0025	142D	60	CALL IN7BIT ; EINLESEN
0027	FF	61	MOV A,R7 ;
0028	4380	62	ORL A,#80H ;SETZE FLAG
002A	AF	63	MOV R7,A ;
002B	3A	64	OUTL P2,A ;
002C	83	65	RET ;
		66	;
		67	;
002D	B800	68	IN7BIT: MOV R7,#0 ;
002F	B807	69	MOV R2,#7 ;
0031	09	70	BIT: IN A,P1 ;
0032	5308	71	ANL A,#1 SHL IRA ;
0034	2F	72	XCH A,R7 ;
0035	E7	73	RL A ;
0036	4F	74	ORL A,R7 ;
0037	2F	75	XCH A,R7 ;
		76	
0038	B816	77	MOV R0,#16H ;
003A	B901	78	MOV R1,#1 ;
003C	1407	79	CALL UPWAIT ;
		80	
003E	EA31	81	DJNZ R2,BIT ;
0040	2F	82	XCH A,R7 ;
		83	REPT IRA ;
		84	RR A ;
		85	ENDM ;
0041	77	86+	RR A ;
0042	77	87+	RR A ;
0043	77	88+	RR A ;
0044	2F	89	XCH A,R7 ;
0045	83	90	RET ;
		91	;
		92	;
		93	END

USER SYMBOLS
 ARBEIT 0000 BIT 0031 ETA 0002 HALTEN 0016 IN7BIT 002D IRA 0003 SCAN 000C TASTE 0017
 UPWAIT 0007 WAIT 001A

ASSEMBLY COMPLETE, NO ERRORS

Components for circuit 4.7.1.

			Ordering code
1	Microcomputer	SAB 8048-P or SAB 8748-D	Q67120-C32-D113 Q67120-C37-D88
1	IR remote control system transmitter	SDA 2008	Q67100-Y503
2	Transistors	BC 238	Q62702-C698
3	Diodes	BA 127D	Q60201-X127-D9
1	Crystal	6 MHz	—
2	Ceramic capacitors	27 pF/63 V	B38062-J6270-G6
1	Ceramic capacitor	10 nF/63 V	B37448-N6103-S2
1	Electrolytic capacitor	1 µF/40 V	B41313-A7105-V
1	Resistor	470 Ω/0.5 W	B51261-Z4471-J1
1	Resistor	15 kΩ/0.5 W	B51261-Z4153-J1
1	Resistor	22 kΩ/0.5 W	B51261-Z4223-J1
1	Resistor	47 kΩ/0.5 W	B51261-Z4473-J1



Components for circuit 4.7

Ordering code	Component	Ordering code
X127-D9	BC 238	Q62702-C698
Q67100-Y503	BA 127D	Q60201-X127-D9
Q67120-C32-D113	6 MHz	—
Q67120-C37-D88	27 pF/63 V	B38062-J6270-G6
B37448-N6103-S2	10 nF/63 V	B37448-N6103-S2
B41313-A7105-V	1 µF/40 V	B41313-A7105-V
B51261-Z4471-J1	470 Ω/0.5 W	B51261-Z4471-J1
B51261-Z4153-J1	15 kΩ/0.5 W	B51261-Z4153-J1
B51261-Z4223-J1	22 kΩ/0.5 W	B51261-Z4223-J1
B51261-Z4473-J1	47 kΩ/0.5 W	B51261-Z4473-J1

4.8 Clock Module with Daily Repeated Alarm

Normally the clock module LZC 085102 B releases an alarm in dependence on date and time. If, however, an alarm repetition is required also at next day the push buttons S_3 and S_4 have to be operated simultaneously.

The operation of both push buttons being by-passed by transistor BC 307 is automatically achieved by the circuit shown in **fig. 4.8**. The transistor is triggered by the trailing edge of the switching signal via the differentiating circuit C_1/R_1 . The capacitor C_2 being charged to level $+V_S$ is discharged and thus transistor BC 307 is blocked.

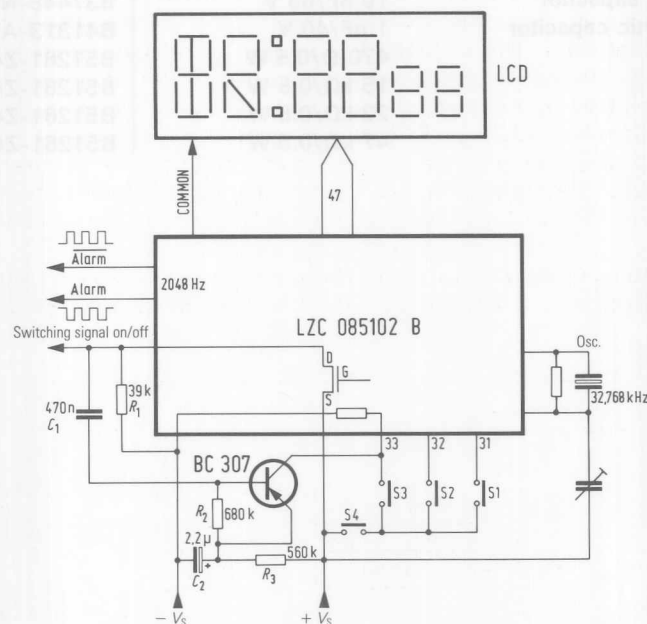


Fig. 4.8

Components for circuit 4.8

		Ordering code
1 Clock module	LZC 085102 B	XQ29-X99
1 PNP-Silicon transistor	BC 307	Q62702-C703
1 MKH-layer capacitor	470 nF/100 V	B32560-D1474-K
1 Electrolytic capacitor	2.2 μF/25 V	B41313-A5225-V
1 Resistor	39 kΩ/0.5 W	B51261-Z4393-J1
1 Resistor	560 kΩ/0.5 W	B51261-Z4564-G
1 Resistor	680 kΩ/0.5 W	B51261-Z4684-G

5. Optoelectronic Circuits

5.1 Four-Digit Display of Program- and Channel-Indication with Serial Data Input for TV Sets

Fig. 5.1.1 shows the circuit of the LED-display driver SDA 2004, which is used to trigger displays with a common cathode. The data is serially applied via the IFO line. The circuit can read two times 8 bit into two different shift registers. The upper shift register is assigned to digits 1 and 2 and the lower one to digits 3 and 4. After the enable line EN is activated the upper shift register takes over a bit at the trailing edge of the shift-clock in conjunction with the clock C_{PR} . Clock C_{KA} is responsible for the lower shift register. With the trailing edge of the enable signal the content of the shift register is temporarily taken over by two other memories. The connected four-digit LED-display is multiplex-operated. The segment-information a to g is applied to the anodes of the LEDs. The various digits are released by means of the selection signals $\overline{D11}$ to $\overline{D14}$. $\overline{D11}$ is assigned to the left display field and $\overline{D14}$ to the right one. An internal clock generator drives the multiplexer and the digit-selection outputs. By connecting the input $4\overline{D1}$ to ground the multiplexer will operate for digit 1 and 2 only. In this case the pulse duty factor of the multiplexer clock is automatically changed.

The LED segments have to be connected via current-limiting resistors with a resistance of approx. 150 Ω each to the SDA 2004 as shown in fig. 5.1.2.

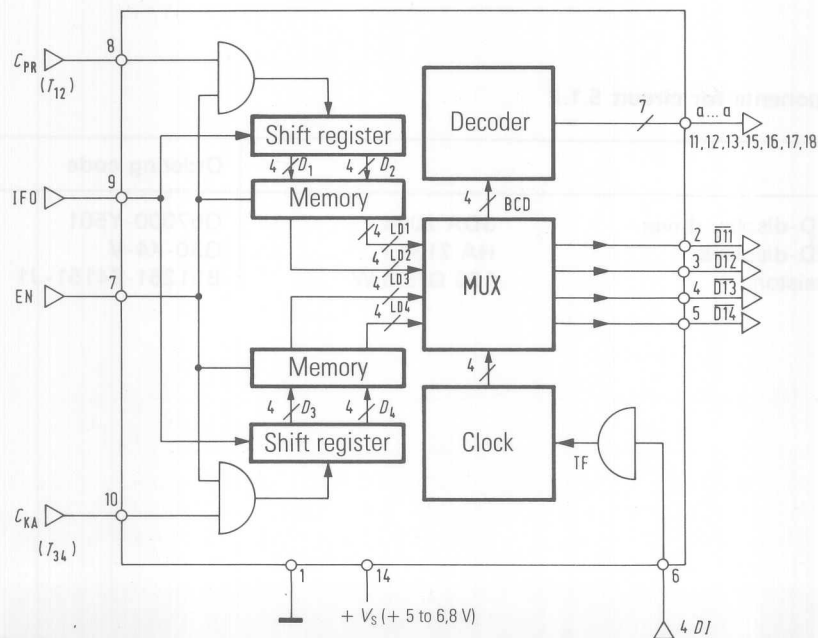


Fig. 5.1.1

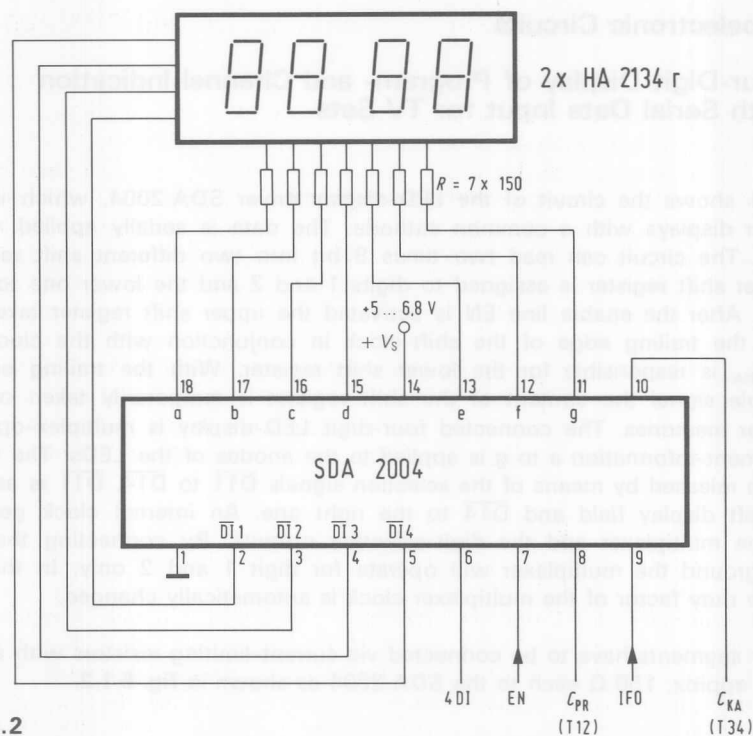


Fig. 5.1.2

Components for circuit 5.1.2

		Ordering code
1 LED-display driver	SDA 2004	Q67000-Y501
2 LED-displays	HA 2134 r	Q30-X4-V
7 Resistors	150 Ω /0.5 W	B51261-Z4151-J1

5.2 Infrared Reflex-Light Barrier with SFH 400 and TDA 4050

The transmitter of this circuit is an IR-LED, type SFH 400, emitting a strongly focussed light beam. TDA 4050 is used as receiving preamplifier. When using a triplet mirror with an area of about 20 cm^2 as reflector, the maximum distance is at least 10 m. The allowed interfering light in lens axis is up to 200 lux (incandescent lamp light). This corresponds to a white surface illuminated at 50 klx over the whole irradiation of the receiver. Emitter and receiver can be placed in the same housing. The circuit is particularly suited for decoding fast changing codes (e.g. running bar patterns) and as light barrier.

Contrary to IR remote controls IR reflex-light barriers require only very narrow emitting and receiving characteristics. Because of the short reaction time required a continuous emitter signal is also needed. Therefore the pulse currents cannot be as high as with remote controls as this operation would exceed the admissible power dissipation.

Transmitter

A circuit consisting of 2 CMOS-NAND-gates (**fig. 5.2.1**) generates a square-wave oscillation with a frequency of approx. 30 kHz. The pulse duty factor is fixed at 4:1. According to experience a good efficiency is achieved herewith. To obtain the desired ratio between pulse duration and pulse space the discharging resistor is partially by-passed by a diode. The 30 kHz-carrier is 1 kHz-modulated by a second pair of gates. When decoding running bar patterns this modulation is not necessary as the object itself will be the source for the modulation.

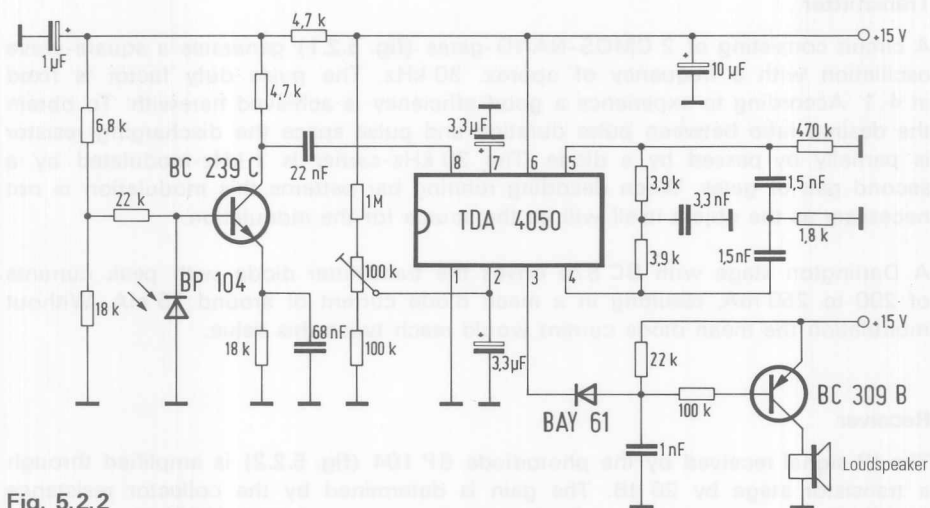
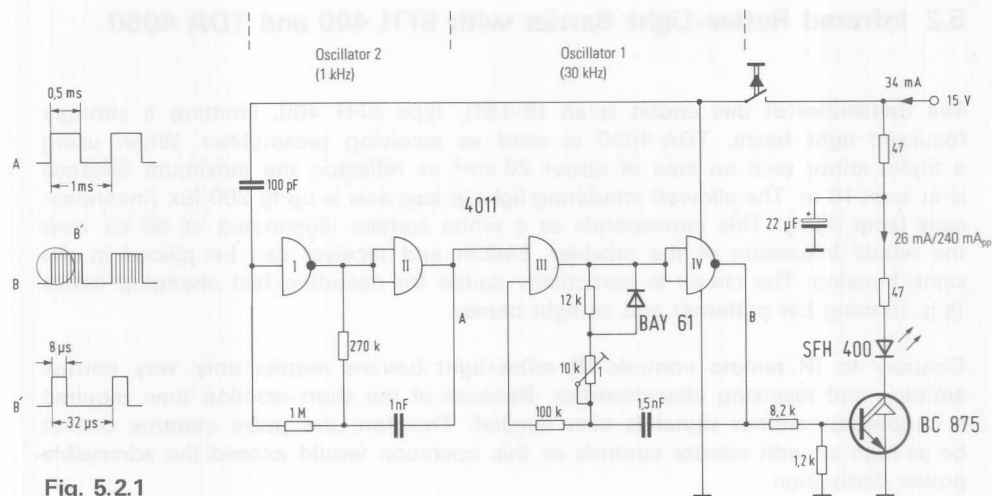
A Darlington stage with BC 875 drives the transmitter diode with peak currents of 200 to 250 mA, resulting in a mean diode current of around 25 mA. Without modulation the mean diode current would reach twice this value.

Receiver

The IR signal received by the photodiode BP 104 (**fig. 5.2.2**) is amplified through a transistor stage by 20 dB. The gain is determined by the collector resistance of $4.7 \text{ k}\Omega$ as well as by the $1.8 \text{ k}\Omega$ -input impedance of TDA 4050. The coupling capacitance of 22 nF and the RC circuit of the emitter reduce drastically low frequency-signals, especially the 50 and 100 Hz-components mainly present in artificial light.

The integrated circuit TDA 4050 has a gain of about 60 dB between input and output. In order to limit the bandwidth, an active filter consisting of a double-T-section is connected between pin 4 and 5. Thus the bandwidth is limited to approx. 10 kHz.

The gain of the TDA 4050 depends on the potential at the control input (pin 2). Normally only a capacitor, being charged to a level of 1 V without signal, is



connected to this terminal. In the circuit, according to fig. 5.2.2, a bias of 1.85 V is set via a voltage divider and the gain is reduced by approx. 20 dB therewith. This is necessary as otherwise, with the increased gain at the output, short-time peaks could result from the control action and would disturb the function. Notwithstanding the adjustment of the basic gain at pin 2 the automatic control is preserved, avoiding an overdrive of the receiver. Due to different charging and discharging resistors of the TDA 4050, downward control is very fast but upward control relatively slow. The controlling time-constant is determined by the capacitor connected to pin 2.

When the input signal at the photodiode exceeds a signal current of 5 nA_{pp} , the output at pin 3 becomes negative.

Acoustic indication and evaluation

Should the incoming signal be acoustically indicated pin 3 has to be connected to an evaluation circuit. It consists for example of a loudspeaker with a transistor BC 309. Besides that with this circuit the limit range can be easily defined as the tone becomes undefined when the maximum range is exceeded.

Optics

For the receiver a collecting lens with a diameter of 15 mm and a focal length of 30 mm is used. Thus an effective receiver area 30 times larger than with photodiode BP 104 is achieved. At the same time the angle of irradiation is restricted to $\pm 3^\circ$. With an increase of the lens diameter the range increases proportionally. But an increase of the focal length at the same time will limit the angle of irradiation.

For the transmitter no additional optic is used, but the parasitic radiation remainder outside the cone becomes inoperative by means of a blackened tubus.

Electrical features

The transmitter must be well shielded against the receiver so that the highly-sensitive receiver input cannot be disturbed. The electrical separation of the lines signals is sufficiently obtained by the filter circuits mentioned.

Technical data

a) Transmitter

Supply current at $V_s = 15\text{ V}$	
unmodulated	60 mA
with 1 kHz-modulation, duty cycle 0.5	34 mA
Carrier frequency (square wave oscillation)	30 kHz
Duty cycle of carrier	0.25
Carrier-pulse-peak radiant intensity	100 mW/sr
Opt. wavelength	950 nm
Cone of radiation (half-angle)	6°

b) Receiver

Supply current at $V_s = 15\text{ V}$	
without load (loudspeaker)	10 mA
load (loudspeaker) only	18 mA
Angle of irradiation with lens	$\pm 3^\circ$
Intermediate frequency	30 kHz
Bandwidth (3 dB)	10 kHz
Min. pulse-peak-radiant-power to diode BP 104	10 nW
Max. modulation frequency	
at standard sensitivity	5 kHz
at reduced sensitivity	10 kHz
Dynamic range	60 dB
Max. interfering light (incandescent lamp light in lens axis)	200 lux

c) Total circuit

Supply current at $V_s = 15\text{ V}$	max. 70 mA ¹⁾
Range with simple triplet mirrors as reflector	
Seize of reflector 20 cm ²	approx. 12 m
Seize of reflector 1000 cm ²	approx. 80 m
Range with top-quality pentaprism as reflector	
seize of reflector 25 cm ²	approx. 20 m

¹⁾ Without modulation and load (loudspeaker)

Components for circuit 5.2

		Ordering code
Transmitter		
1 NAND-gate	4011 PC	Q67100-H792
1 Darlington-Transistor	BC 875	Q62702-C853
1 IR-transmitter diode	SFH 400/II	Q62702-P783
1 Silicon-diode	BAY 61	Q62702-A389
1 Capacitor	100 pF	B38066-J6101-G6
1 Capacitor	1 nF	B37062-A6102-K6
1 Capacitor	1.5 nF	B37062-A6152-K
1 Electrolytic capacitor	22 μ F	B41283-C8226-T
2 Resistors	47 Ω /0.5 W	B51261-Z4470-J1
1 Resistor	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	8.2 k Ω /0.5 W	B51261-Z4822-J1
1 Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	270 k Ω /0.5 W	B51261-Z4274-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1
1 Potentiometer	10 k Ω	
Receiver		
1 IC	TDA 4050 B	Q67000-A1373
1 Transistor	BC 239 C	Q62702-C282
1 Transistor	BC 309 B	Q62702-C289
1 Photodiode	BP 104	Q62702-P84
1 Diode	BAY 61	Q62702-A389
1 Capacitor	1 nF	B37062-A6102-K6
2 Capacitors	1.5 nF	B37062-A6152-K
1 Capacitor	3.3 nF	B37062-A6332-K
1 Capacitor	22 nF	B37449-F6223-S2
1 Capacitor	68 nF	B32509-A683-M
1 Electrolytic capacitor	1 μ F	B41313-A7105-V
2 Tantalum capacitors	3.3 μ F	B45170-E4335-M
1 Electrolytic capacitor	10 μ F	B41313-A7106-T
1 Resistor	1.8 k Ω /0.5 W	B51261-Z4182-J1
2 Resistors	3.9 k Ω /0.5 W	B51261-Z4392-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	6.8 k Ω /0.5 W	B51261-Z4682-J1
2 Resistors	18 k Ω /0.5 W	B51261-Z4183-J1
2 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
2 Resistors	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	470 k Ω /0.5 W	B51261-Z4474-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1
1 Potentiometer	100 k Ω	

5.3 Simple Infrared Remote Control with Low Current Consumption

For remote-controlled switch operation a very simple circuit is only needed. The infrared signal consists of a 20 kHz burst with a duration of approx. 1 ms. To reduce the interference by ambient light and flashes, an integrating circuit is connected to the receiver, which will only supply a trigger pulse after having been applied by a series of pulses.

Transmitter

A 20 kHz-oscillator consisting of two CMOS-NAND gates (fig. 5.3.1) is used. As long as gate 2 has L-level, the oscillation is interrupted. After pressing key T, H-potential is applied to the input of gate 1 as well as to the output of gate 2 and the oscillator starts operating. After a certain time, determined by the time constant of the C_1R_1 -circuit, the voltage at the input of gate 1 drops below the minimum H-level threshold and thus the oscillation is interrupted. The time constant of R_1C_1 -circuit is dimensioned for a burst-length of 1 ms. The 1 nF-capacitor, connected to output of gate 1, suppresses pulse spikes during turn-on.

Due to the oscillation at the output of G_4 , the Darlington transistor BC 875 is periodically conductive. The transmitter diodes, type LD 271 are operated at peak currents of up to 1 A. The energy is supplied during 1 ms by the 470 μ F-capacitor. Its voltage drops by a value of 1 V during the burst.

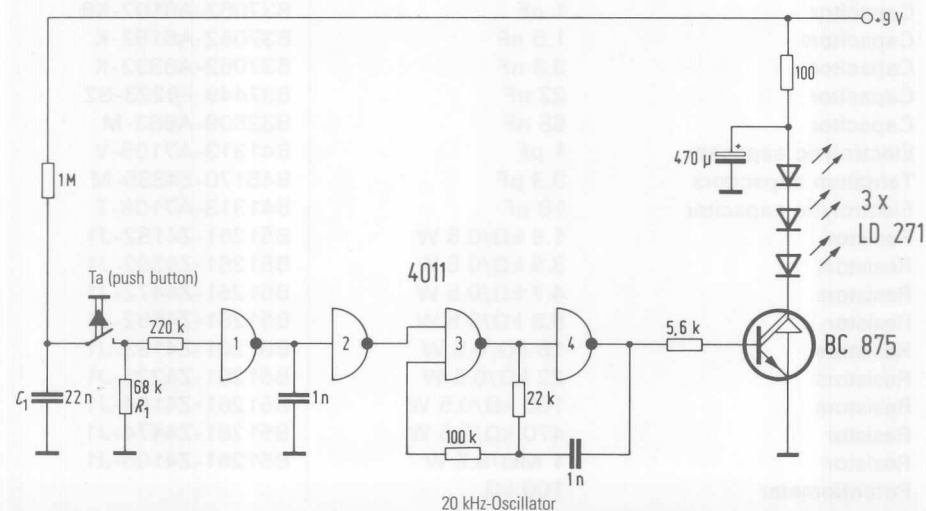


Fig. 5.3.1

Receiver

The photodiode BP 104 with integrated IR filter is used as load with a resistance of $56\text{ k}\Omega$ (fig. 5.3.2). At normal ambient light this resistance is low enough to generate no voltage drop. The next stage is an emitter follower with an input impedance of approx. $1\text{ M}\Omega$. In conjunction with the second stage a gain of 100 is achieved. The dc operating point is controlled by means of an inverse feedback. By the next two stages, being also part of the inverse feedback circuit, the signal is further amplified by a factor of approx. 100.

The input signal, amplified totally by a factor of 10,000 is supplied to an integrated rectifier circuit. At each pulse the 10 nF -capacitor is charged by a certain voltage depending on the capacitances relations (680 pF and 10 nF). As soon as the threshold of the transistor, being connected to the rectifying circuit is reached, a pulse with a positive switching edge is generated. It is steepened by means of four inverters. This edge triggers the following JK-flip-flop 4027 operating as a monoflop. At its output a defined pulse is available for triggering the following flip-flop 4027. In this case antivalent outputs are used to drive a red or a green LED.

Technical data

Transmitter

Supply voltage	9 V
Pulse width (single pulse)	approx. 1 ms
Carrier frequency	approx. 20 kHz
Peak current	approx. 1 A

Receiver

Supply voltage	9 V
Supply current (without LED)	2 mA
Intermediate frequency	approx. 20 kHz
Gain	approx. 80 dB
Range	$\geq 15\text{ m}$

Components for the following circuits

		Ordering code
Transmitter (5.3.1)		
1 C-MOS quad NAND-gate	4011 PC	Q67100-H792
3 Transmitter diodes	LD 271	Q62703-Q148
1 Transistor	BC 875	Q62702-C853
2 MKT-capacitors	1 nF/100 V	B32510-D6102-K
1 Ceramic capacitor	22 nF/63 V	B37449-F6223-S2
1 Al-electrolytic capacitor	470 μ F/10 V	B41283-A3477-T
1 Resistor	100 Ω /0.5 W	B51261-Z4101-J1
1 Resistor	4.6 k Ω /0.4 W	B54311-A462-F402
1 Resistor	22 k Ω /0.5 W	B51261-Z4223-J1
1 Resistor	68 k Ω /0.5 W	B51261-Z4683-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	220 k Ω /0.5 W	B51261-Z4224-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1
Receiver (5.3.2)		
1 C-MOS JK-flip-flop	4027 PC	Q67100-J536
1 C-MOS Hex-inverter	4049 DC	Q67100-H980
1 Photodiode	BP 104	Q62702-P84
3 Transistors	BC 238	Q62702-C698
2 Transistors	BC 308	Q62702-C704
2 Germaniumdiodes	AA 118	Q60101-X118
1 LED	LD 57 C	Q62703-Q100-S4
1 LED	LD 52 C	Q62703-Q160
2 Ceramic capacitors	10 nF/63 V	B37449-N6103-S2
1 Ceramic capacitor	22 nF/63 V	B37449-F6223-S2
1 MKT capacitor	47 nF/100 V	B32510-D1473-K
1 Tantalum capacitor	3.3 μ F	B45170-E4335-M
1 Al-electrolytic capacitor	220 μ F/10 V	B41283-C3227-T
1 Switch		
2 Resistors	680 Ω /0.5 W	B51261-Z4681-J1
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	1.5 k Ω /0.5 W	B51261-Z4152-J1
1 Resistor	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	15 k Ω /0.5 W	B51261-Z4153-J1
1 Resistor	47 k Ω /0.5 W	B51261-Z4473-J1
2 Resistors	56 k Ω /0.5 W	B51261-Z4563-J1
1 Resistor	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	150 k Ω /0.5 W	B51261-Z4154-J1
1 Resistor	650 k Ω /0.5 W	B51261-Z4651-G
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1

5.4 Solar Cell Generator for Exposure Control in Cameras without Moving Parts

Exposure meters normally work with a moving coil instrument. With a field effect liquid crystal display and a solar generator with two photovoltaic cells, type BPY 64 a fully electronic light control without mechanical moving parts can be realized. The reversal point of the indicator is reached at an illumination of 100 lux (colour temperature of 2850 K). Thus exposure-time display for low-priced cameras is possible.

Circuit description

A basic requirement is an oscillator which starts oscillating at a voltage below 100 mV. Two photovoltaic cells, type BPY 64, feed a blocking oscillator with transistor AC 121 VII as shown in **fig. 5.4**. Because of the low photo-electric voltage available at low illuminations a germanium transistor with a low threshold voltage has to be used. In operation, the transistor is at first conductive so that a magnetic field can be built up in the primary winding of the transformer Tr. Through the secondary winding a reverse voltage is induced to the base circuit which turns off the transistor. At this moment the magnetic field of the coil collapses. The potential difference between collector and base is momentarily approx. 5 V at the break-down point of the liquid crystal display. To avoid a too strong damping of the base circuit by the capacitor of the display, two diodes are connected in series to the LCD. The pulse duration of the blocking oscillator signal is mainly defined by the self-inductance and self-capacitance of the coil, while the repeating frequency depends on the time constant of the base circuit. The optimum output voltage is achieved at a repeating frequency of approx. 3 kHz. The oscillations start at a collector voltage V_{CE} of -60 mV and a mean current I_C of 30 μ A.

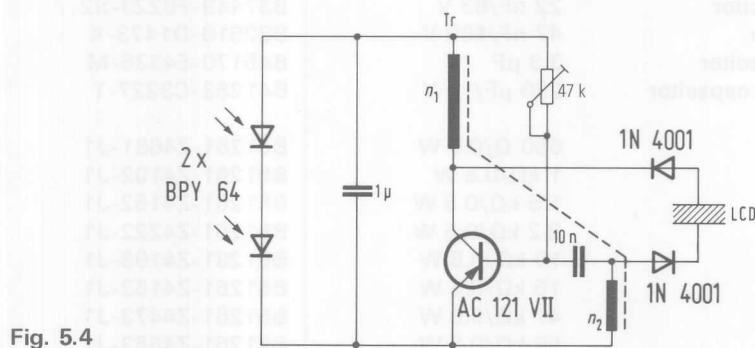


Fig. 5.4

Components for circuit 5.4

		Ordering code
2 Photovoltaic cells	BPY 64 P	Q60215-Y67
1 Transistor	AC 121 VII	Q60103-G121
2 Silicon diodes	1 N 4001	C66047-Z1306-A21
1 LCD	(as required)	
1 MKT-capacitor	10 nF/63 V	B32509-A103-M
1 Electrolytic capacitor	1 μ F/25 V	B43286-C4105-T
1 Potentiometer	47 k Ω	B58042-Z473-M320
1 Transformer, consisting of pot core according to		B65541-K000-R030

Coil data of blocking oscillator

Pot core 14×8 , material N30 (B65541-K0000-R030)

$N_1 = 666$ turns, 0.07 ECu, $N_2 = 333$ turns, 0.07 ECu, $L_1 = 1.8$ H



5.5 Flashing Diode with Low Current Consumption

For battery-operated devices a clear 'on' indication with low current consumption is often needed. It should remind a user to turn off the measuring instrument after he has finished. The usual current consumption of flashing diodes is of 20 mA. When using the circuit according to **fig. 5.5** a supply current of 200 μA is needed. The current can be reduced even further if the flashing frequency is reduced. With short but strong light pulses at longer intervals, a well perceptible warning signal is achievable at low power consumption.

The voltage to be supervised charges a 47 μF -capacitor via a 22 k Ω -resistor. When reaching a threshold defined by the input characteristic and the two diodes, type LD 35, (or several Si-diodes in series) transistor BC 875 is turned on and LED LD 32C emits light. Because of the current consumption the voltage decreases at capacitor C_1 . After about 1 ms the input of the first inverter has reached L-level and the switching transistor blocks again. C_1 is charged again and the process is repeated. To reduce the current consumption of the CMOS circuit an additional 22 k Ω -resistor is connected to mains.

As the characteristic of the CMOS circuit strongly determines the threshold, the switching point may eventually have to be corrected by means of further series-diodes or by leaving a diode out.

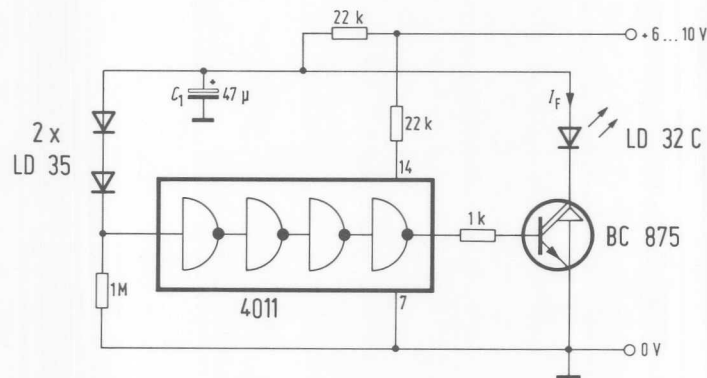


Fig. 5.5

Technical data

Supply voltage V_s	9 V
Supply current I_s	200 μ A
Frequency of flashing	1.6 Hz
Peak current of LED	100 mA
Duty cycle	0.002

Components for circuit 5.5

4 NAND-gates (used as inverters)	4011 PC	Q67100-H792
1 Transistor	BC 875	Q62702-Q853
1 LED	LD 32 A	Q62703-Q194
2 LEDs	LD 35 A	Q62703-Q118-S1
1 Electrolytic capacitor	47 μ F/40 V	B41283-D7476-T
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
2 Resistors	22 k Ω /0.5 W	B51261-Z4223-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1

5.6 Control Circuit for Photovoltaic Cell-Panel SFH 140-36¹⁾

In practical applications photovoltaic cells are normally operated with buffer batteries. The control circuit should prevent an overloading of the buffer accumulator when the load current being required is too low. The circuit shown in **fig. 5.6** consists of a Schmitt-trigger and following buffer stage which drives the switching relay. The Schmitt-trigger has a hysteresis of 0.25 V. It can be varied by the resistance of the resistor R_1 . The switch-off voltage of the device is of 14 V, the turn-on voltage is 13 V. Thus an overloading of the accumulator is avoided for sure. As soon as the switch-off voltage of the Schmitt-trigger is reached (it can be adjusted by means of potentiometer P_1), contact r cuts off the buffer battery from the photovoltaic cell-panel.

The rectifier BSY 26 avoids discharging of the buffer battery via the photovoltaic cell if, because of too low illumination, the voltage of the photovoltaic cell-panel is lower than the buffer battery one.

Supply current of the control circuit is

at $V_s = 12$ V: $I_s = 4.1$ mA and

at $V_s = 14$ V: $I_s = 10$ mA.

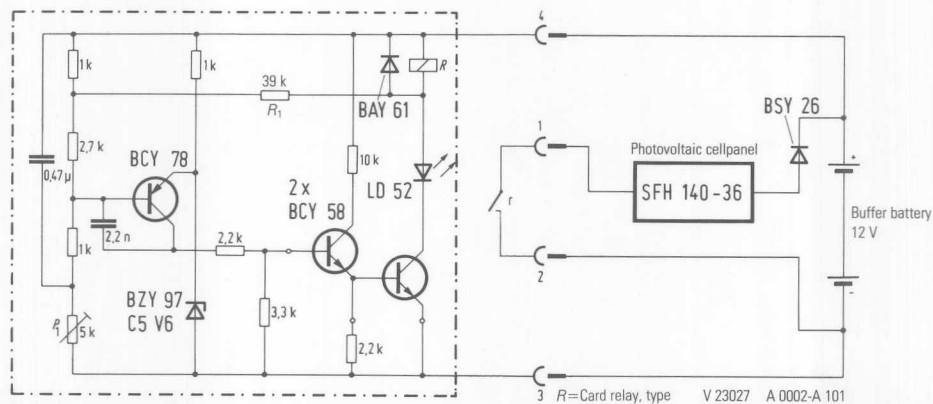


Fig. 5.6

¹⁾ If additional information for more complex control circuits is required please contact our sales department.

Components for circuit 5.6

		Ordering code
1 Solar cell panel	SFH 140-36	Q62702-P842-F1
2 Transistors	BCY 58	Q60203-Y58
1 Transistor	BCY 78	Q60203-Y78
1 LED	LD 52 A	Q62703-Q157
1 Z-diode	BZX 97 C5V6	Q62702-Z1229-F82
1 Schottky-diode	BYS 26	C67047-Z1325-A1
1 Diode	BAY 61	Q62702-A389
1 Ceramic capacitor	2.2 nF/63 V	B37062-A6222-K6
1 Electrolytic capacitor	0.47 μ F/63 V	B41313-A8474-V
1 Card relay		V23027-A0002-A101
1 Potentiometer	5 k Ω	—
3 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
2 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	2.7 k Ω /0.5 W	B51261-Z4272-J1
1 Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
1 Resistor	39 k Ω /0.5 W	B51261-Z4393-J1



5.7 Automatic Readjustment for Light Barriers

Very often the problem with applications of light barriers has to be solved in that a continuous alarm is released without interruption of the light beam due to ageing effects of the used phototransistors and LEDs. The circuit shown in **fig. 5.7** compensates the radiant power decrease of the LED, caused by ageing effects, by an automatic readjustment of the diode current (up to max. 100 mA). Thus a constant output voltage at the phototransistor is guaranteed. Potentiometer P_1 determines the starting current for the LED with 50 mA.

The emitter of the phototransistor is connected to the inverted input of the operational amplifier. If the output voltage at the phototransistor decreases, the TAA 761 A increases the current for the LED. It is limited to a maximum of approx. 100 mA by a 68- Ω -resistor.

Components for circuit 5.7.

			Ordering code
1 Operational amplifier	TAA 761 A		Q67000-A522
1 Phototransistor	BPX 43 II		Q62702-P16-S2
1 GaAs-LED	SFH 400 II		Q62702-P783
1 Ceramic capacitor	100 pF		B37979-J5101-J
1 Electrolytic capacitor	10 μ F/6.3 V		B41313-A2106-V
1 Potentiometer	250 k Ω		B58042-Z224-M620
1 Resistor	68 Ω		B51261-Z4680-J1
1 Resistor	10 k Ω		B51261-Z4103-J1
1 Resistor	100 k Ω		B51261-Z4104-J1
1 Resistor	1.5 M Ω		B51261-Z4155-J1

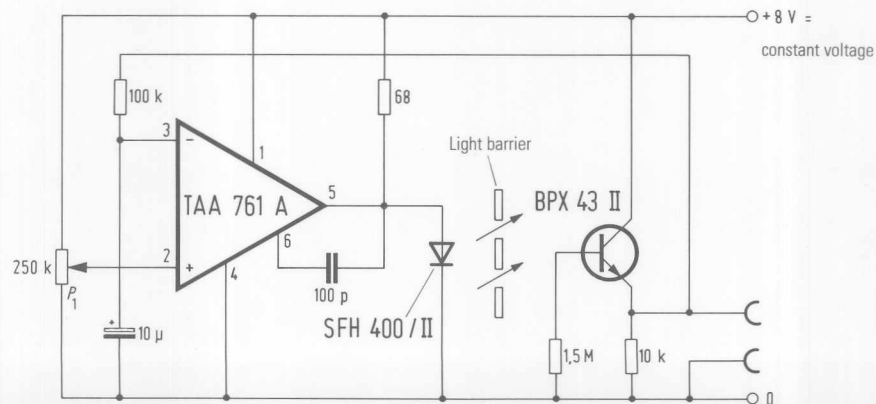


Fig. 5.7

6. Circuits for Testing, Controlling and Regulating

6.1 Characteristic—Linearization of Silicon Temperature Sensor KTY 10

The relatively linear temperature characteristic R_T of the new-developed silicon temperature sensor KTY 10 can be further linearized by an additional resistor. It is connected in series if the sensor is operated with a constant-voltage source and in parallel if the KTY 10 is driven by a constant-current source.

Fig. 6.1.1 shows the theoretical characteristic voltage V_T versus temperature T . For achieving a deviation minimum the operating point T_W is in the middle of the considered measuring range. The corresponding resistance optimum R_{OPT} is derivable from the R-T-characteristic shown in fig. 6.1.2. In practice the voltage divider, consisting of temperature sensor and series resistor R_{OPT} , is loaded by the input resistance of the following circuit as demonstrated in fig. 6.1.3. Therefore the series resistance R_{OPT} has to be corrected by the following relation:

$$R_{OPT}^* = \frac{R_{OPT}}{1 - \frac{R_{OPT}}{R_E}}$$

The V_T -T-characteristic becomes less steep but the point of inflection is not influenced when R_{OPT} is substituted by R_{OPT}^* .

Operation with a constant-current source is simpler. In this case a 6.8 k Ω -resistor, considering already the input resistance of the following circuit, is connected in parallel to the temperature sensor. Only a very small linearization error of the function $V_T(T)$ is achieved and it is ± 1 °C over a temperature range from -50 °C to $+150$ °C. Between 0 °C and 100 °C the error is ± 0.2 °C. The resulting temperature coefficient TK is 0.56%/K. The sensor current I_T should not exceed 1.5 mA to avoid self-heating.

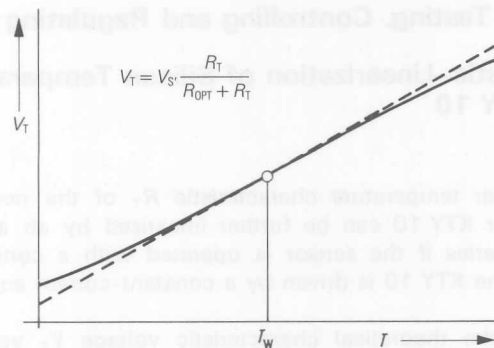


Fig. 6.1.1

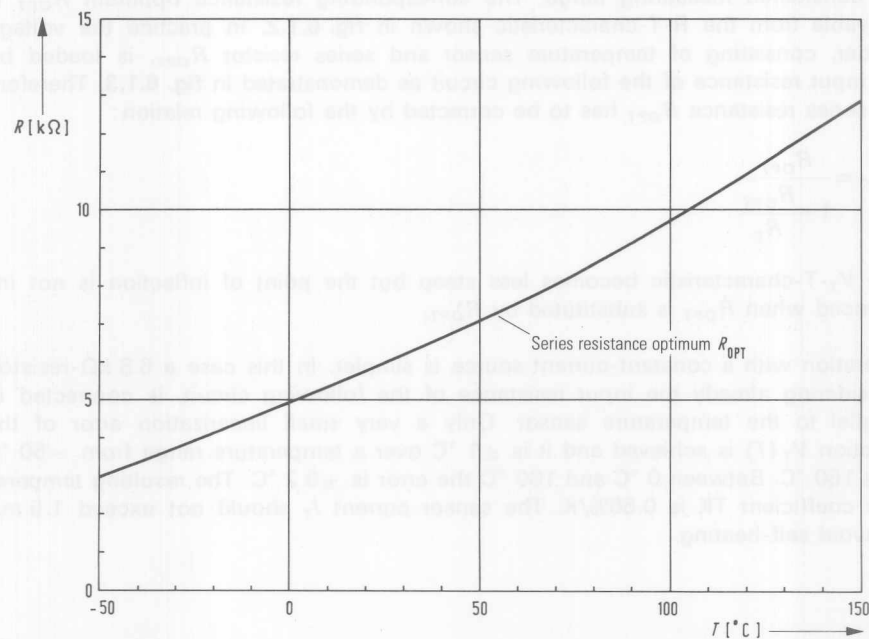


Fig. 6.1.2

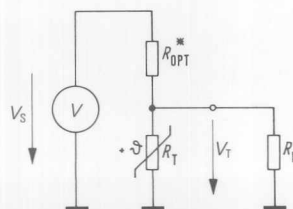


Fig. 6.1.3

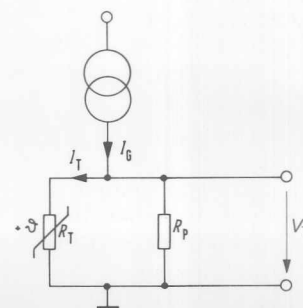


Fig. 6.1.4

6.2 Circuit of Analog Signal Processing for Temperature Measurement with Si-Sensor KTY 10

Fig. 6.2.1 shows a bridge circuit for analog signal processing. The temperature sensor KTY 10 and the 6.8 k Ω -resistor are part of one bridge arm and the two resistors R_1 and R_2 belong to the second one. The bridge voltage is regulated by z-diode 1N5731D. This measure is necessary to operate independently on line losses because of line resistances.

Transistor BC 307 is part of the feedback circuit for the operational amplifier TAA 761. It matches also the load R_L to the IC. The circuit is dimensioned for a current between 0 to 20 mA. The dependence of the output current on ambient temperature is shown in fig. 6.2.2. The deviation referred to the standard curve is demonstrated in fig. 6.2.3. The linearity error is 1‰ from the total measuring range.

The accuracy is influenced by:

- resistance tolerances
- tolerance of the z-diode voltage
- variations of the supply voltage ΔV_s
- temperature dependency of the z-diode voltage
- temperature characteristic of the resistors.

The upper and lower curves shown in fig. 6.2.3 demonstrate the extreme values at resistance deviations of 1%. The error maximum is obtained at $T=100$ °C assuming the current I is adjusted to zero at a temperature $T=40$ °C by means of potentiometer R_p . As the upper and lower curves are nearly linear the relative error is constant over the total measuring range.

However, the errors caused by the tolerances of z-diode voltage and by the variations of supply voltage ΔV_s have to be considered to get the absolute error at $T=100$ °C. The mentioned values have to be added and a total $\pm 2\%$ -accuracy of full-scale value is attained if the following operating limits are considered.

Technical data of the current source

Supply voltage	V_s	11.5 to 12.5	V
Output current	I	0 to 20	mA
Open-loop current at $I=0$ mA	I_{so}	70	mA
Supply current at $I=20$ mA	I_s	91	mA
Z-voltage	V_z	$6.2 \pm 1\%$	V
Z-impedance	Z_{zT}	10	Ω
TC of z-voltage	TC	+2.3	mV/K
Ambient temperature	T_{amb}	0 to +70	°C
Measuring temperature	T	+40 to +100	°C
Output voltage at R_L	V_{Lmax}	8	V
Load maximum	R_{Lmax}	400	Ω
Error at $T_{max}=100$ °C	F_A	± 2	°C

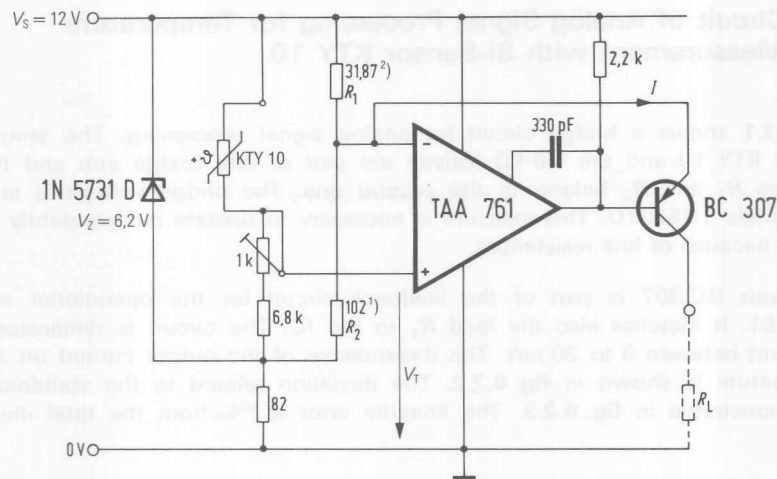


Fig. 6.2.1

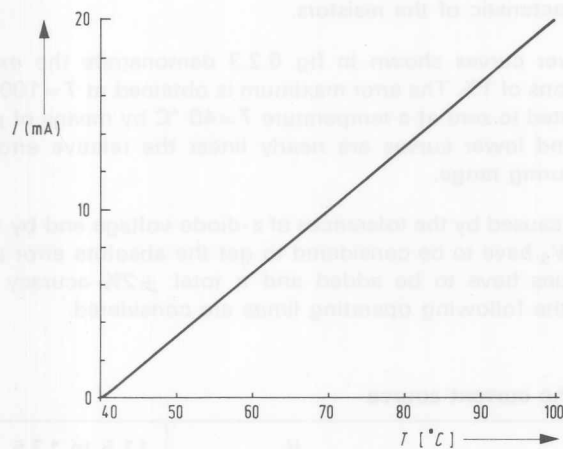


Fig. 6.2.2

¹⁾ $27 \Omega + 75 \Omega$

²⁾ $56 \Omega || 75 \Omega$

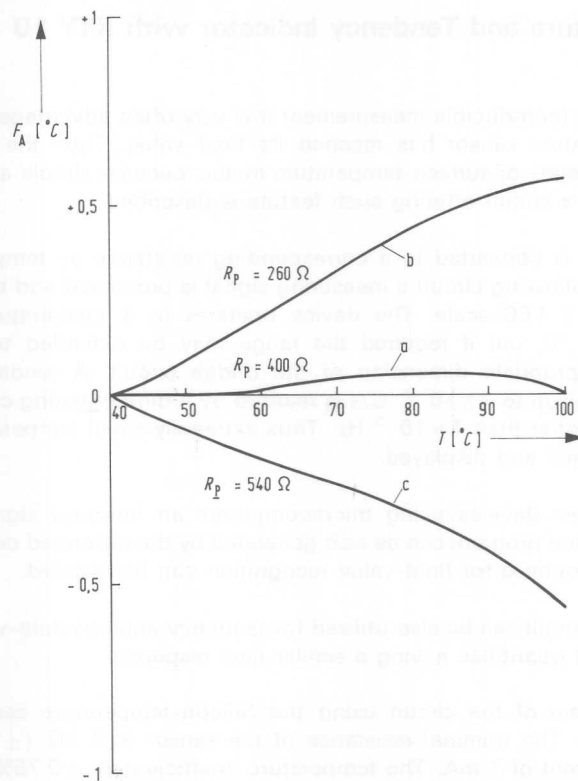


Fig. 6.2.3

Components for circuit 6.2

			Ordering code
1	Temperature sensor	KTY 10 A	Q62705-k1
1	Operational amplifier	TAA 761	Q67000-A224
1	Transistor	BC 307	Q62702-C703
1	Z-diode	1N5731D	
1	Ceramic capacitor	330 pF/50 V	B37979-J5331-J
1	Resistor	82 Ω /1.1 W/1%	B54321-B4820-F2
2	Resistors	75 Ω /1.1 W/1%	B54321-B4750-F2
1	Resistor	2.2 k Ω /0.5 W/5%	B51261-Z4222-J1
1	Resistor	6.8 k Ω /1.1 W/1%	B54321-B4682-F2
1	Resistor	27 Ω /1.1 W/1%	B54321-B4270-F2
1	Resistor	56 Ω /1.1 W/1%	B54321-B4560-F2

6.3 Temperature and Tendency Indicator with KTY 10

For accurate and reproducible measurement it is very often advantageous to indicate that the temperature sensor has reached its final value. Thus the application of clinical thermometers or surface-temperature meters become simple and convenient. In the following a circuit offering such feature is described.

The temperature is converted to a corresponding resistance by temperature sensor KTY 10. In the following circuit a measuring signal is processed and the temperature is indicated on a LED-scale. The device operates in a temperature range from $+18\text{ }^{\circ}\text{C}$ to $+41\text{ }^{\circ}\text{C}$, but if required the range may be extended to $-50\text{ }^{\circ}\text{C}$ and $+150\text{ }^{\circ}\text{C}$ by appropriate dimension of the bridge circuit. A tendency indication with a solution of up to $3 \times 10^{-3}\text{ }^{\circ}\text{C/s}$ is realized by a differentiating circuit operating at frequencies higher than $1 \times 10^{-3}\text{ Hz}$. Thus extremely small temperature variations are safely indicated and displayed.

For automatic test devices using microcomputers an interrupt signal for starting the data acquisition program can be also generated by the described circuit. Therefore many software routines for final-value recognition can be avoided.

In principle the circuit can be also utilized for tendency and absolute-value indication of other physical quantities having a similar time response.

The block diagram of the circuit using the Silicon-temperature sensor KTY 10 A shows **fig. 6.3.1**. The nominal resistance of the sensor is $2\text{ k}\Omega$ ($\pm 1\%$) at $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ and a current of 1 mA . The temperature coefficient is $+0.75\%/K$. An output voltage V_A being proportional to temperature is supplied from the amplifier to two UAA 180 which drive an LED-array. The temperature is indicated by steps of $1\text{ }^{\circ}\text{C}$ per each LED in a range between $+18\text{ }^{\circ}\text{C}$ and $+41\text{ }^{\circ}\text{C}$.

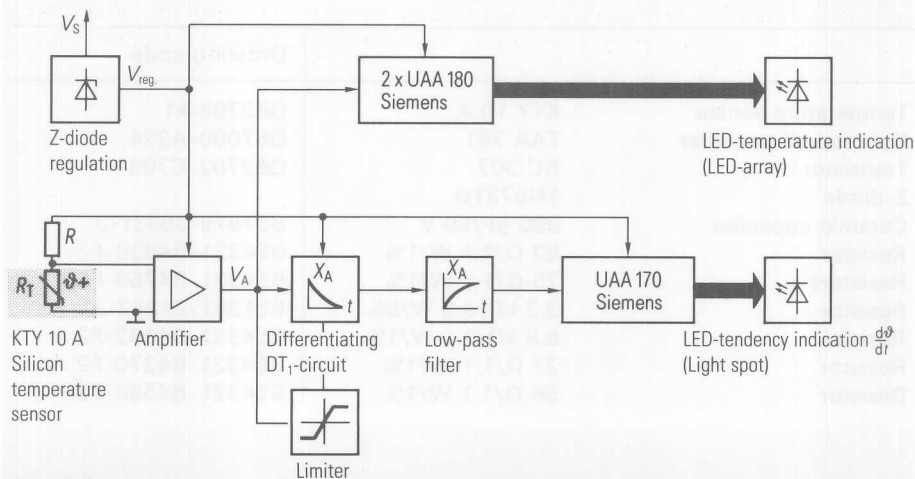


Fig. 6.3.1

The voltage V_A is differentiated for indicating the tendency of temperature variations. A low-pass filter suppresses voltage pulse-spikes from the mains. The indicator consisting of several LEDs is operated by driver IC UAA 170. Saturation effects are avoided by the limiter connected to the differentiating circuit. Therefore unrequired delays do not occur when the voltage V_A exceeds admissible levels.

A regulation circuit incorporating a chain of z-diodes keeps the mean voltage of the differentiator constant and also supplies a regulated voltage for the measuring bridge and the LED driver ICs.

Z-diode regulation

The regulation circuit including 4 Z-diodes D_1 to D_4 has an internal resistance of $5.5\ \Omega$ referred to its output. The regulated output voltage differs only by 0.1% at input voltage variations of $\Delta V_S = 1\text{ V}$.

Measuring amplifier

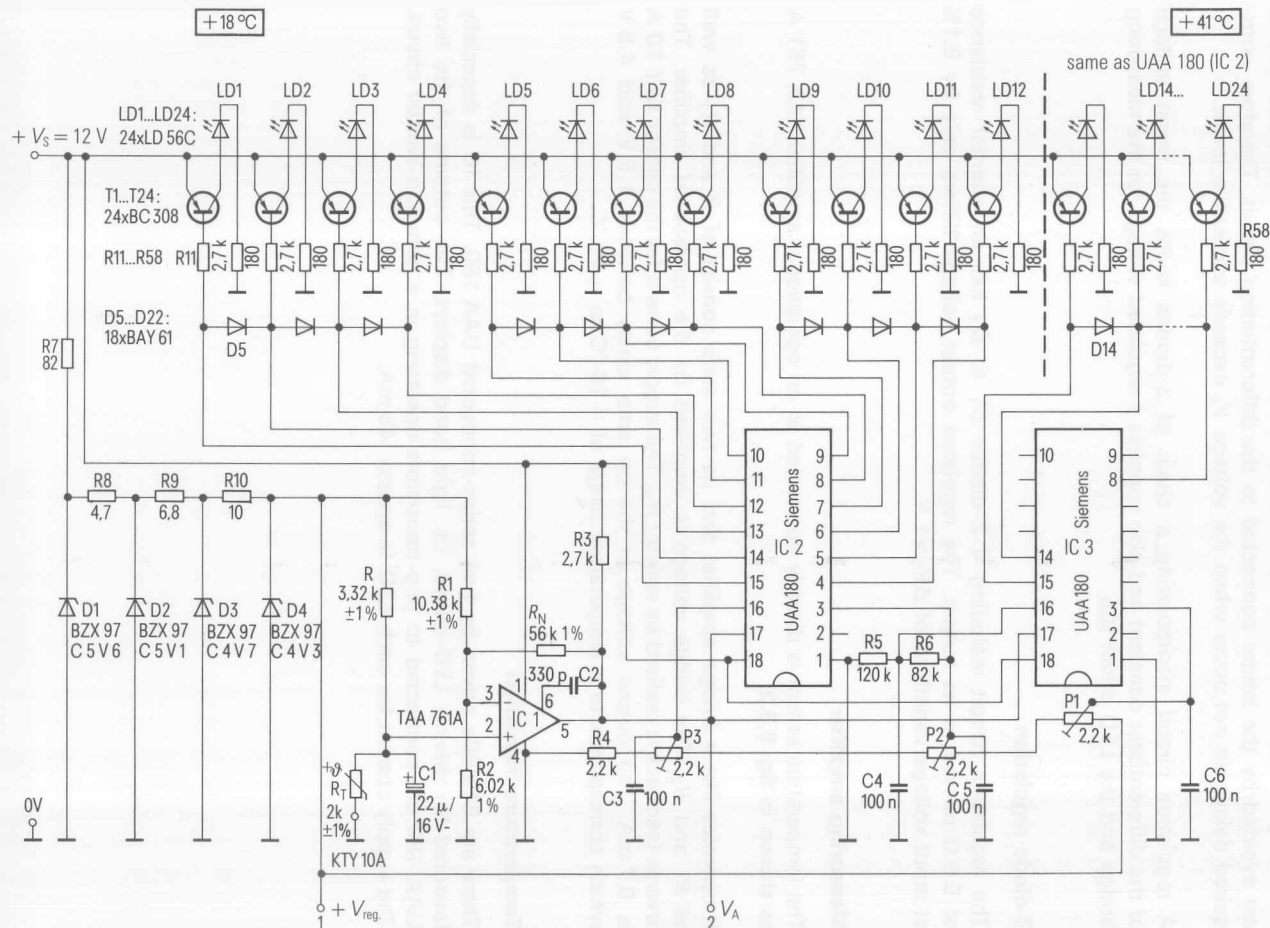
The temperature sensor is directly connected to an operational amplifier TAA 761 A as shown in **fig. 6.3.2**.

It operates like a bridge amplifier and its two arms consist of R and R_T as well as R_1 and R_2 . The bridge voltage is amplified by the operational amplifier. The reverse feedback is realized by resistor R_N . The supply current for the sensor KTY 10 A is 0.7 mA. The output voltage of the op amp varies between 1.5 V and 4.5 V which corresponds to a temperature range of $+18\text{ }^\circ\text{C}$ to $+41\text{ }^\circ\text{C}$.

Temperature indication

There are 24 LEDs driven by two series-connected UAA 180. This IC is especially favoured for driving LED-arrays, i.e. light band displays. The outputs of the two UAA 180 are connected to pnp-transistors operating in a common-emitter circuit. The supply current for each LED is approx. 45 mA.

6.3.2



Components for circuit 6.3.2.

		Ordering code
1	Operational amplifier TAA 761 A	Q67000-A522
2	Driver ICs for LED-arrays UAA 180	Q67000-A1104
24	Silicon-AF-transistors BC308B	Q62702-C286
24	LEDs LD56C	Q62703-Q165
1	Silicon Z-diode BZX97/C5V6	Q62702-Z1229-F82
1	Silicon Z-diode BZX97/C5V1	Q62702-Z1228-F82
1	Silicon Z-diode BZX97/C4V7	Q62702-Z1227-F82
1	Silicon Z-diode BZX97/C4V3	Q62702-Z1226-F82
18	Silicon switching diodes BAY61	Q62702-A389
1	Ceramic multi-layer capacitor 330 pF	B37979-J5331-J
4	Ceramic multi-layer capacitors 100 nF, $\pm 10\%$	B37987-J5104-K
1	Tantalum electrolytic capacitor 22 μ F, 16 V	B45181-A2226-M
1	Metal-layer resistor 3.32 k Ω , 0.4 W, $\pm 1\%$	B54311-A332-F202
1	Metal-layer resistor 6.81 k Ω	B54311-A682-F102
	0.4 W, $\pm 1\%$	
1	Metal-layer resistor 3.57 k Ω	B54311-A352-F702
	0.4 W, $\pm 1\%$	
2	Metal-layer resistors 3.01 k Ω , 0.4 W, $\pm 1\%$	B54311-A302-F102
1	Metal-layer resistor 56 k Ω , 0.4 W, $\pm 1\%$	B54311-A563-F3
3	Carbon-layer resistors 0.5 W, $\pm 5\%$	B51261-Z4...J1
3	Carbon-layer resistors 1 W, $\pm 2\%$	B51276-A2...G
	KARBOWID (small-size power resistors)	
48	Carbon-layer resistors 0.5 W, $\pm 5\%$	B51261-Z4...J1
1	Silicon temperature sensor KTY 10 A	Q62705-K1
3	Spindle potentiometers 2.2 k Ω , 0.75 W	B58612-Z222-M310

Potentiometers P_1 to P_3 are responsible for calibration of the thermometer as well as for adjusting the offset voltage of IC2 and IC3.

The adjustment procedure is as follows: First the upper temperature limit of $+41\text{ }^{\circ}\text{C}$ is set by potentiometer P_1 . In this case all LEDs emit light also LED no. 24. Then the lower temperature limit of $+18\text{ }^{\circ}\text{C}$ is adjusted by P_3 . In this case only LED no. 1 emits light. P_2 is responsible for adjusting the change-over from IC2 to IC3. P_2 is set at $T = +29\text{ }^{\circ}\text{C}$ in that all LEDs emit light also LED no. 12. This last adjustment finishes the procedure. If accurate temperature standards are not available, the temperature sensor KTY 10 (R_T) can be replaced by a potentiometer. In this case the temperature variation is simulated by resistance changes. At a nominal resistance for R_T of $2\text{ k}\Omega$ at $+25\text{ }^{\circ}\text{C}$ it follows

- $+41\text{ }^{\circ}\text{C}$: $2245.4\text{ }\Omega$ (upper limit),
- $+29\text{ }^{\circ}\text{C}$: $2060.0\text{ }\Omega$,
- $+18\text{ }^{\circ}\text{C}$: $1897.1\text{ }\Omega$ (lower limit).

Tendency indication

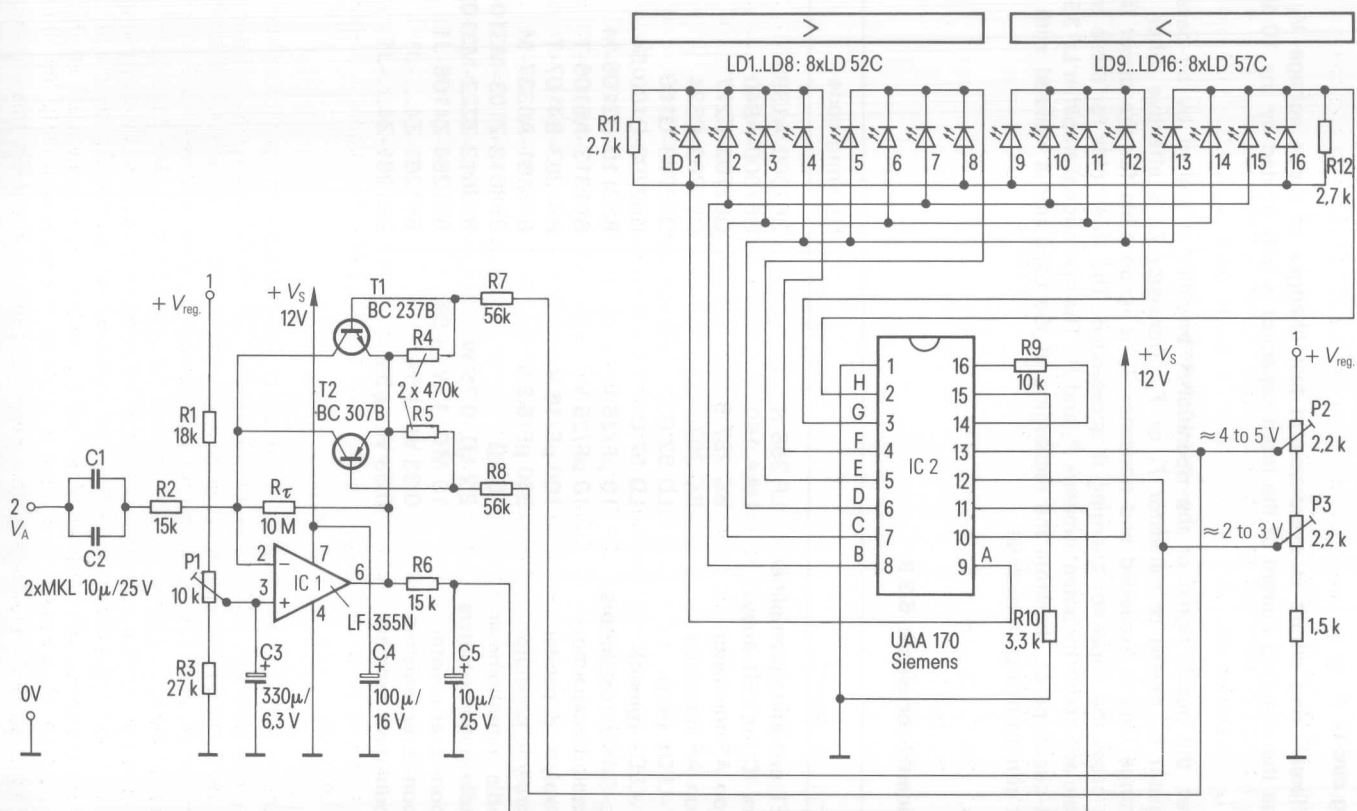
The differentiating circuit (see **fig. 6.3.3**) must have a time constant which is 20 times greater than 20 s to guarantee that voltage increases, corresponding to temperature rises with time constants of up to $\tau = 20\text{ s}$, are safely differentiated.

Capacitances of C_1 and C_2 are limited by the leakage current. Therefore an active circuit with an operational amplifier is necessary for realizing such high time constants at $R_T = 10\text{ M}\Omega$. Because of the high resistance of the feedback resistor R_T the JFET-operational amplifier LF 355 N has to be used. The mean voltage is adjusted to a level of 3 V by potentiometer P_1 to operate the op amp in the admissible common-mode range. The $15\text{ k}\Omega$ -resistor R_2 decreases the signal for the inverted input of the differentiating op amp. The output voltage variation is 0.6 V with reference to the mean voltage when the input voltage varies with a speed of 3 mV/s .

Short-time pulse spikes from the mains are suppressed by a low-pass filter. It features a cutoff frequency of $f_g = 1\text{ Hz}$ and therefore the effective signal is practically not attenuated.

The tendency range indicated by light spots is adjustable by potentiometers P_2 and P_3 connected to IC2, UAA 170. From the 16 diodes only one is operated. The supply current is 45 mA . It is determined by the load resistances. LD1 to LD8 are responsible for indicating an increasing tendency whereas LD9 to LD16 indicate a decreasing one. In the neutral position both diodes LD8 and LD9 are to emit light of the same intensity. The adjustment is realized by potentiometer P_1 . During the adjustment procedure the input of the differentiating circuit (V_A) should not be connected to the amplifier but has to be grounded by a $2.7\text{ k}\Omega$ -resistor (see **fig. 6.3.2**). Thus a stable indication is attained. The indication limits are symmetrically adjusted with reference to the mean voltage by potentiometers P_2 and P_3 . If the range is tightened up the indication sensitivity will be increased and the change-over from a diode to another will be smoother.

Fig. 6.3.3



Limiting circuit

The differentiating circuit is overdriven at fast changes of input voltage V_A . In this case the charging current of the input capacitor is only limited by the 10 M Ω -resistor.

However, the output signal of the operational amplifier is limited by by-passing this resistor by means of transistor T_1 or T_2 . Transistor T_1 is effective when the lower range limit is exceeded and transistor T_2 is responsible for the upper limit. In both cases the capacitor charging is accelerated. The thresholds for these transistors are adjustable by potentiometers P_2 and P_3 . The operational amplifier LF 355 N is short-circuit proof, therefore the recharging of the capacitor is realized with the highest current being admissible.

Components for circuit 6.3.3

		Ordering code
1 J-FET operational amplifier	LF 355 N	Q67000-A1399
1 Driver IC for LED-arrays	UAA 180	Q67000-A940
1 Silicon AF-transistor	BC 237 B	Q62702-C277
1 Silicon AF transistor	BC 307	Q62702-C324
8 TSN-LEDs (red)	LD 52 C	Q62703-Q160
8 GaP-LEDs (green)	LD 57 C	Q62703-Q100-S4
2 MKL-(MKU-)capacitors	10 μ F/25 V	B32110-D3106-M
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Electrolytic capacitor	100 μ F/16 V	B41283-B4107-T
1 Electrolytic capacitor	330 μ F/6.3 V	B45181-A0337-M
1 Spindle potentiometer	10 k Ω	B58612-Z103-M310
2 Spindle potentiometers	2.2 k Ω , 0.75 W	B58612-Z222-M310
1 Carbon-layer resistor	10 M Ω , 1 W, $\pm$ 5%	B51264-Z4106-J1
8 Carbon-layer resistors	0.33 W, $\pm$ 5%	B51261-Z4...-J1
4 Carbon-layer resistors	0.33 W, $\pm$ 5%	B51261-Z4...-J1

6.4 Resistance-to-Frequency Converter for Temperature Measurement Using Temperature Sensor KTY 10

For digital signal processing the resistance of a temperature sensor is not measured but it is favourably converted to a frequency. Thus TTL-counters or microprocessors can be driven directly. The advantage of this method is in that only a data line to the microprocessor is required besides the ground line, assuming that the microprocessor incorporates an internal counter.

In the circuit shown in **fig. 6.4** the $R(T)$ -characteristic of the temperature sensor is linearized by using a series resistor R_V connected to the sensor. The divider output voltage V_i directly depends on temperature. It is applied to the voltage-to-frequency converter, which converts V_i to a charging current I_L by means of a controlled current source. V_{CT} is compared with V_{R1} and the capacitor C_T is discharged via transistor T_2 when $V_{CT} = V_{R1}$.

The voltage-controlled current source is realized by operational amplifier TAA 761 in conjunction with transistor T_1 . As long as V_{CT} is lower than V_{R1} the output of comparator TCA 315 is at the level of the power supply voltage. Transistor T_2 is non-conductive and capacitor C_T is charged by I_L . When V_{CT} increases and reaches the threshold V_{R1} the comparator becomes conductive and its output voltage is now 0.2 V. Transistor T_2 is driven into saturation by a strong base current flowing via resistor R_3 . Now the capacitor C_T is discharged via T_2 . The frequency of

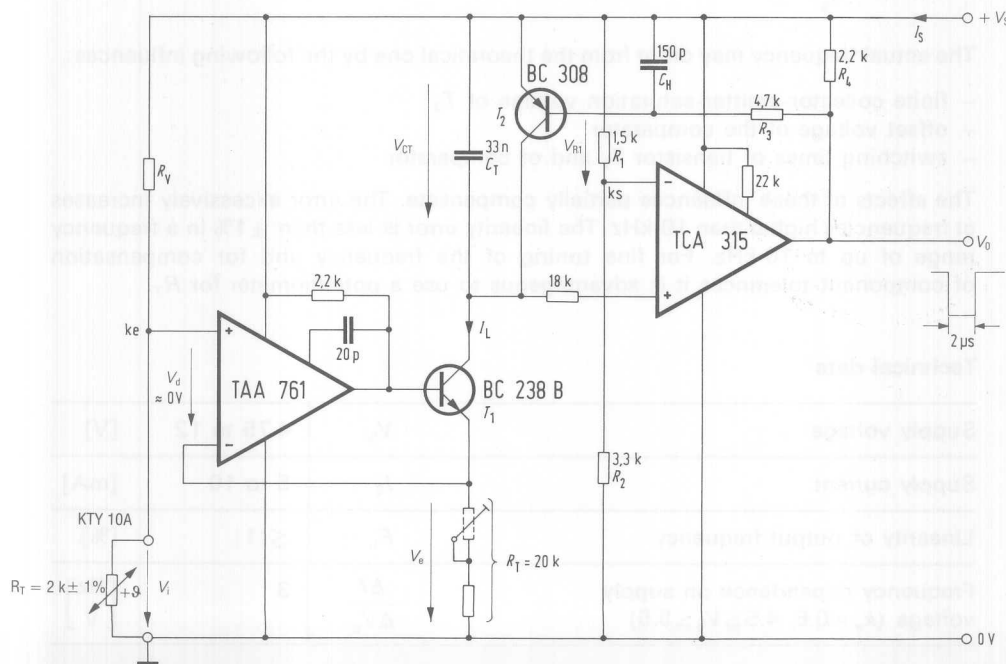


Fig. 6.4

the output voltage is:

$$f = \frac{I_L}{C_T \times V_{CT}}$$

with

$$k_e = \frac{R_{Th}}{R_V + R_{Th}}$$

and

$$k_s = \frac{R_1}{R_1 + R_2}, \text{ it follows}$$

$$f = \frac{k_e}{R_T \times C_T \times k_s}.$$

The output voltage depends on the time constant $\tau = R_T \times C_T$ as well as of the divider ratios k_e and k_s , but it does not rely on the supply voltage V_s . Therefore a power supply regulation is not necessary.

The output frequency changes are determined by the possible variations of k_e , which are

$$0.2 \leq k_e \leq \frac{V_s - 2V}{V_s}.$$

The actual frequency may differ from the theoretical one by the following influences:

- finite collector-emitter-saturation voltage of T_2
- offset voltage of the comparator
- switching times of transistor T_2 and of comparator.

The effects of these influences partially compensate. The error excessively increases at frequencies higher than 10 kHz. The linearity error is less than $\pm 1\%$ in a frequency range of up to 10 kHz. For fine tuning of the frequency and for compensation of component-tolerances it is advantageous to use a potentiometer for R_T .

Technical data

Supply voltage	V_s	4.75 to 12	[V]
Supply current	I_s	5 to 10	[mA]
Linearity of output frequency	F_L	$\leq 1 $	[%]
Frequency dependence on supply voltage ($k_e = 0.6, 4.5 \leq V_s \leq 5.5$)	$\frac{\Delta f}{\Delta V_s}$	3	$\left[\frac{\text{Hz}}{\text{V}} \right]$

The output signal is TTL-compatible if $V_s = 5 \text{ V}$.

Components for circuit 6.4

			Ordering code
1	Operational amplifier	TAA 761	Q67000-A224
1	Operational amplifier	TCA 315	Q67000-A1004
1	Transistor	BC 238	Q62702-C698
1	Transistor	BC 308	Q62702-C704
1	Temperature sensor	KTY 10A	Q62705-K1
1	Styroflex-capacitor	20 pF/160 V	B31063-B1200-H
1	Styroflex-capacitor	150 pF/160 V	B31063-B1151-H
1	MKT-layer capacitor	33 nF/63 V	B32509-A333-M
1	Resistor	1.5 k Ω /0.5 W	B51261-Z4152-J1
2	Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1	Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
1	Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
1	Resistor	18 k Ω /0.5 W	B51261-Z4183-J1
1	Resistor	22 k Ω /0.5 W	B51261-Z4223-J1



6.5 Excess Temperature Indicator for Cooling Water Using Blinking Display

Very often it is convenient to draw a driver's attention to the excess temperature of the cooling water by a blinking display. This can be realized by a bridge circuit, consisting of the voltage divider with resistors R_1 and R_2 as well as of the NTC-resistor and the hot-wire instrument. The temperature sensor being in thermal contact to the cooling water is connected in series to the hot-wire meter indicating the temperature. The voltage E^- being applied to the negative input of the op amp is the sum of the voltage at point B and the forward voltage of diode 1N4148. Voltage E^+ being supplied to the positive input of the op amp becomes smaller when the voltage at bridge point A decreases, i.e. when the cooling water becomes hotter. As long as voltage E^+ is higher than E^- the output transistor of the op amp is turned off and the LED, type LD 41, does not emit light. But when voltage E^+ is lower than E^- the op amp is turned on by the influence of the feedback voltage of the R_4/R_5 -divider. Now the LED emits light. The voltage E^+ is simultaneously decreased by influence of the feedback resistor R_5 . The capacitor C_2 is discharged via resistor R_3 as long as the voltage E^- becomes smaller than E^+ . In this case the output transistor of the op amp is switched off. This turn-off is improved by the influence of feedback resistor R_5 . The LED is also switched off. Now capacitor C_2 is charged again via resistor R_3 and thus a continuous sweep-operation is realized, as long as a certain cooling water temperature ($\approx 90^\circ\text{C}$) is exceeded.

Notice

The supply voltage V_s^+ has to be the same as the one for the hot-wire meter, indicating the temperature as shown in **fig. 6.5**. Generally this voltage is regulated to a level of $\approx 10\text{ V}$.

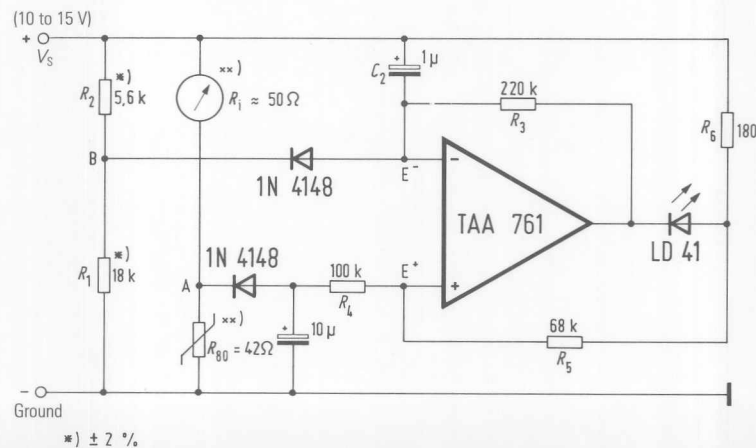


Fig. 6.5

Components for circuit 6.5

		Ordering code
1	Operational amplifier	TAA 761
1	LED	LD 41 A
2	Switching diodes	1N4148
1	Electrolytic capacitor	1 μ F/40 V
1	Electrolytic capacitor	10 μ F/25 V
1	Resistor	180 Ω /0.5 W
1	Resistor	5.6 k Ω /0.5 W
1	Resistor	68 k Ω /0.5 W
1	Resistor	100 k Ω /0.5 W
1	Resistor	220 k Ω /0.5 W
1	Resistor	18 k Ω /0.5 W

6.6 Microcomputer-Controlled Air-Conditioning System

In the following the principles of wired as well as wireless remote-controlled air-conditioning systems are described.

Fig. 6.6.1 shows the circuit for a wireless remote-controlled system. The transmitter uses the key-board decoder SDA 2008. There are 62 instructions possible, but only 6 are utilized.

The circuit for the wired remote-controlled device is shown in **fig. 6.6.2**. It also operates with IC SDA 2008. The key information is serially transmitted to the receiver decoder SDA 2007 via a single line. The system status being set by the microcomputer of the control device can be read in a shift register via a serial three-line bus (data, dataline-enable, clock). Thus a repeating possibility is realized. The shift registers drive the corresponding LEDs.

As against conventional solutions the wiring elaborateness is reduced from 21 to 6 connecting lines by using the remote-control IC SDA 2008. Besides the cost reduction the thinner cable is more flexible and handier, too.

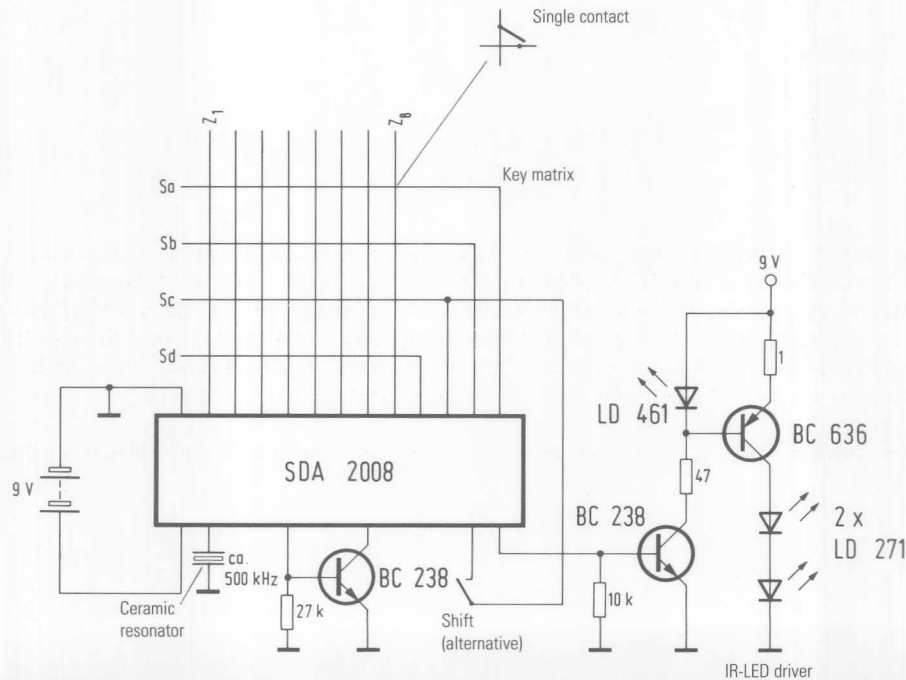


Fig. 6.6.1

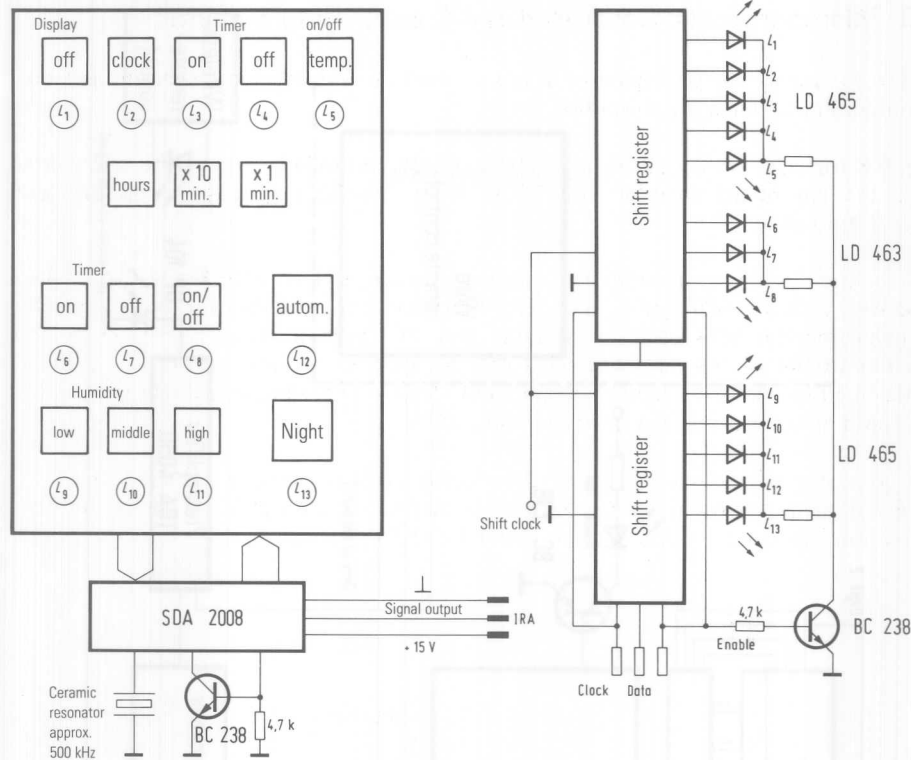


Fig. 6.6.2

Fig. 6.6.3 shows the block-diagram. The key board, built up as a SCAN-matrix, and the display driver SDA 2004 are connected directly to the microcomputer. The remote-controlled receiver SDA 2007 is connected to the SAB 8048 via a serial interface. By an additional circuit requiring only a few components the display driver can be modified in that an "F" is displayed at the second digit as it is common for the 10-step indication of the fan speed.

The different functions of the device are indicated in the circuit shown in fig. 6.6.2.

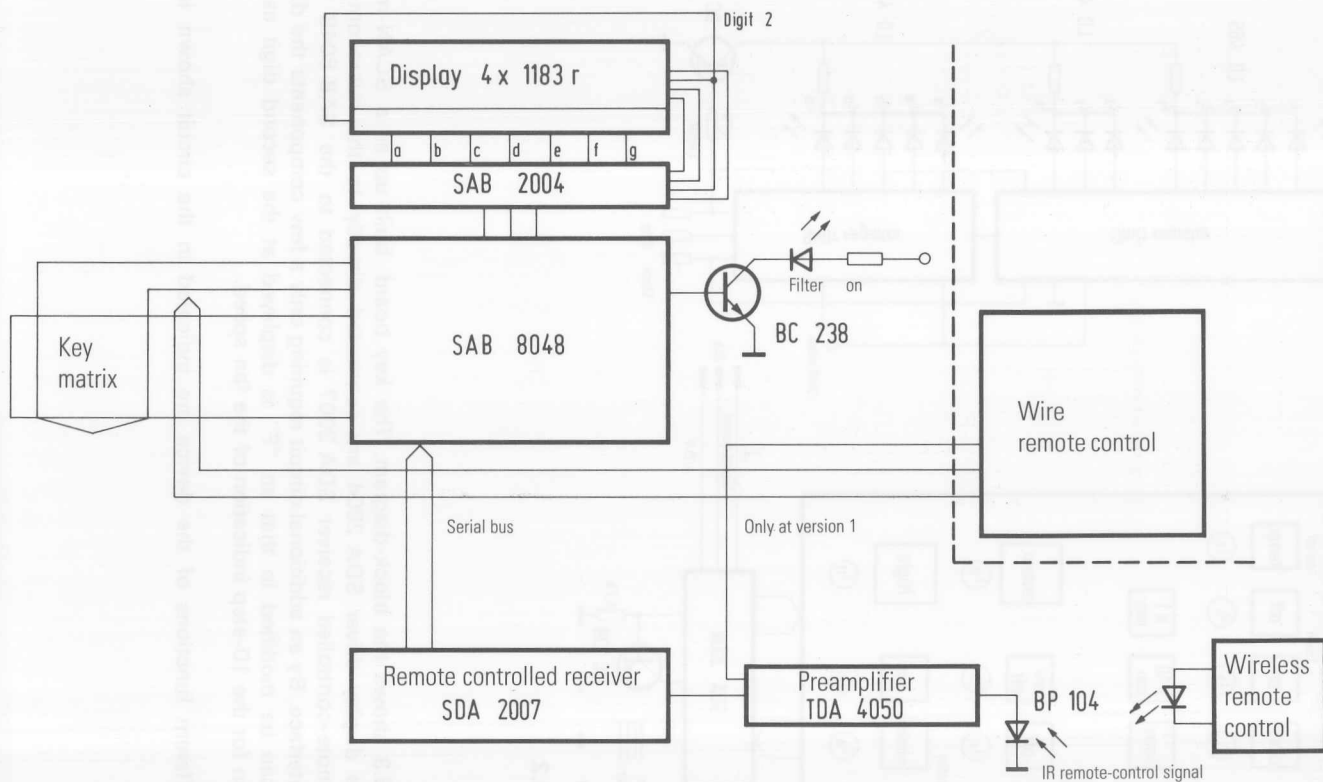


Fig. 6.6.3

Components for circuit 6.6

			Ordering code
1	Microcomputer	SAB 8048-P	Q67120-C32-D113
1	Preamplifier	TDA 4050 B	Q67000-A1373
1	Remote control system receiver	SDA 2007	Q67100-Y504
2	Remote control system transmitters	SDA 2008	Q67100-Y503
1	Display driver	SDA 2004	Q67000-Y501
5	Transistors	BC 238	Q62702-C698
1	Transistor	BC 636	Q68000-A3365
2	IR-LEDs	LD 271	Q62703-Q148
1	IR photodiode	BP 104	Q62702-P84
2	LED-arrays	LD 465	Q62703-Q83
1	LED-array	LD 463	Q62703-Q81
1	LED	LD 461	Q62703-Q79
1	Resistor	1 Ω /0.4 W	B54311-Z5010-G1
1	Resistor	47 Ω /0.5 W	B51261-Z4470-J1
1	Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1	Resistor	27 k Ω /0.5 W	B51261-Z4273-J1

6.7 Hygrometer with Digital Indication

Fig. 6.7 shows a circuit of a hygrometer with liquid crystal display indicating the relative humidity as percentage. The sensor is capacitively realized (KHY 10). It determines the duration of pulses generated by a monostable multivibrator, which is driven by a 1 kHz-oscillator. At zero humidity the width of the monostable multivibrator pulse is equal to the half-wave duration of the 1 kHz-oscillator signal. At a humidity of 100% the monostable multivibrator pulse length is 20% longer. Both signals are supplied to an EXOR-gate, which generates an output being the difference of both inputs. Its duration is between 0 and 100 μ s in dependence on the humidity. The width of the difference pulse is determined by counting of pulses with a higher frequency. This is realized by applying both difference pulse and 200 kHz-needle-pulse to an AND-gate. Its output only supplies needle-pulses if a difference pulse is also applied to the input.

As the difference pulses have a length maximum of 100 μ s and as the needle pulses have a distance of 5 μ s the counting resolution is relatively inaccurate. Therefore all needle pulses from approx. 500 difference pulses are counted by applying a pulse signal with a frequency of 1 Hz to the third input of the AND-gate. Thus a gate time of 500 ms is realized.

The 1 kHz-oscillator is not to be synchronized with the 200 kHz-one to achieve a high accuracy for measuring the pulse duration. Therefore two separate-operating oscillators are used. Besides that it is important that the 200 kHz-frequency and the gate-time of 500 ms have a good time relation. This is guaranteed by dividing the frequency of the 200 kHz-oscillator signal by a divider chain in that a 1 Hz-signal is finally generated.

At a humidity of 100% a maximum of 10^4 pulses are available at the output of the AND-gate. As a two-segment display is required for humidity indication the number of pulses has to be divided by 100 and to be applied to a two-decade BCD-counter. Its output is applied to a liquid crystal display via a memory-decoder driver. At the end of the 500 ms-time a control pulse is generated by a special circuit shown in fig. 6.7 (see left side below). By this control pulse the content of the counter is stored in a memory. Then counter as well as predivider are reset.

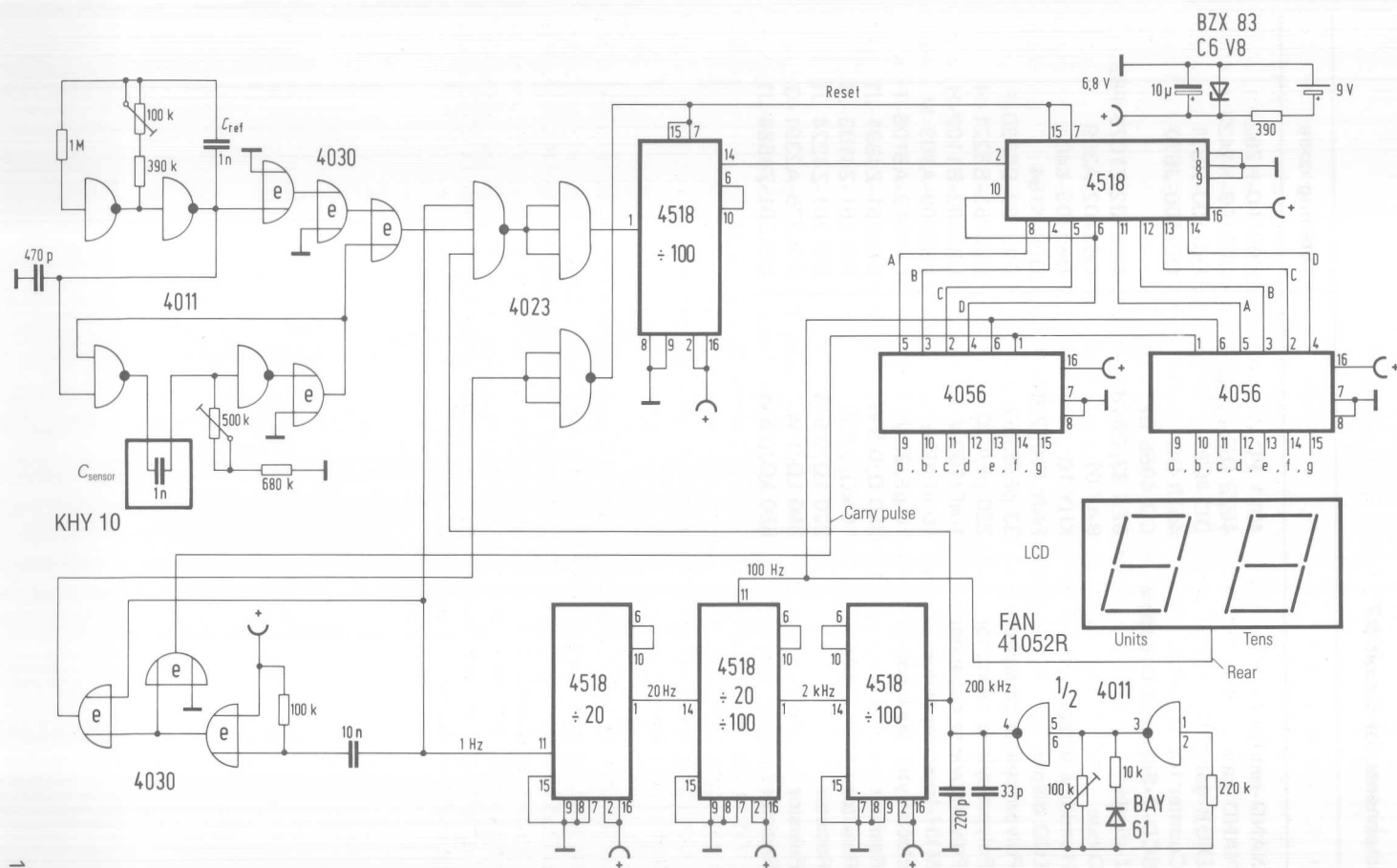


Fig. 6.7

Components for circuit 6.7

		Ordering code
2 NAND-gates	4011 PC	Q67100-H792
1 NAND-gate	4023 DC	Q67100-H1433
2 EXOR-gates	DC 4030	Q67100-H871
5 Counter ICs	4518 DC	Q67100-J670
2 BCD-7-Segment-Decoders	CD 4056 BF	
1 Z-diode	BZX 83/C6V8	Q62702-Z1073-F82
1 Diode	BAY 61	Q62702-A389
1 Humidity sensor	KHY 10	Q62705-K40
1 LCD display	FAN 41052 R	Q28-X194
1 Polypropylene capacitor	33 pF/630 V	B33063-B6330-F
1 Polypropylene capacitor	220 pF/630 V	B33063-B6221-H
1 Polypropylene capacitor	1 nF/160 V	B33063-B1102-H
1 MKH-layer capacitor	10 nF/63 V	B32509-A103-M
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Resistor	390 Ω /0.5 W	B51261-Z4391-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	220 k Ω /0.5 W	B51261-Z4224-J1
1 Resistor	390 k Ω /1 W	B51276-A2391-G
1 Resistor	680 k Ω /0.5 W	B51261-Z4684-J1

6.8 Threshold Switch with TCA 105

The IC TCA 105 is a threshold switch, which is well suited for sensors switching amplifiers, voltage-control devices, time circuits, light barriers and especially for proximity-switching applications. The TCA 105 features an internal voltage regulation. Therefore an operation in a supply voltage range of 4.5 V to 30 V is possible. Besides that this IC comprises an oscillator stage, a threshold switch and two anti-valent output stages. Thus TTL-compatibility as well as a relatively high output current of 50 mA for direct driving of relays are guaranteed.

Fig. 6.8 shows the TCA 105 used in a light barrier or with an opto coupler. When the light beam is interrupted the relay pulls up. Besides the phototransistor no external components are additionally required for the receiver circuit. The photocurrent depends on temperature. But this effect is nearly compensated at a constant LED-current by the oppositely oriented input current of the TCA 105. The operating point is constant in a supply voltage range between 4.5 V and 30 V. The hysteresis can be increased by resistor R , if required.

Very often a galvanic separation of two current loops is necessary. In this case LED and phototransistor of circuit 6.8 have to be replaced by an opto coupler. Thus a galvanic separation with a high dc voltage isolation is realized. The LED of the coupler can be directly driven by microcomputers, TTL- or LSL-gates. In this case the supply current is less than 1 mA.

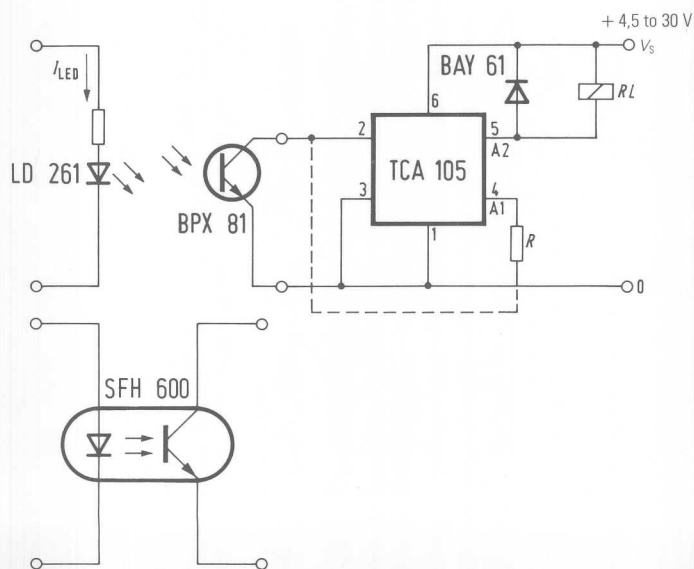


Fig. 6.8

Components for circuit 6.8

		Ordering code
1 Threshold-switch IC	TCA 105	Q67000-A527
1 LED	LD 261 IV	Q62703-Q66
1 Phototransistor	BPX 81	Q62702-P20
1 Diode	BAY 61	Q62702-A389
1 Relay (with driver current <50 mA)		
For potential separation:		
Opto coupler	SFH 600 I	Q68000-A4861



6.9 Rotational Speed Control with TCA 955

DC motors are favourably used for electronic drives, the rotational speed of which has to be constant even if supply voltage, load and temperature vary. The advantage is in that dc motors can be controlled by its armature voltage. In this case a speed controlling IC, type TCA 955, is utilized. It operates in accordance to the principle of a keyed control and corresponds to a dc-voltage converter, which reduces the supply voltage nearly without any losses.

The armature is controlled by width-modulated pulses at twice the frequency of the tachogenerator. During the pulse space the energy, being stored in the armature inductor, is decreased, i.e. the motor nearly operates with a direct current.

If the electric motor time-constant is too low the switching oscillator can be used. It is keyed at high frequencies.

As against conventional control circuits this device offers the following two essential advantages:

- the rotational speed control is independent of the amplitude of the tachogenerator voltage,
- at higher supply voltages the efficiency of the control is improved. Therefore the operating time is extended when the motor is operated with a battery.

Fig. 6.9.1 shows the circuit of a speed control for a dc motor with the following characteristics:

nominal supply voltage 4.5 V,
nominal power consumption 0.6 W,
armature resistance 6 Ω ,
6 pole pairs.

The electric motor time-constant is $T_{\text{mot}} > \frac{30}{(n \times p)}$ at a nominal rotational speed of 2200 rpm. The circuit operates without a switching oscillator and a few external components are only required. **Fig. 6.9.2** demonstrates the control accuracy and the current saving in dependence on the supply voltage.

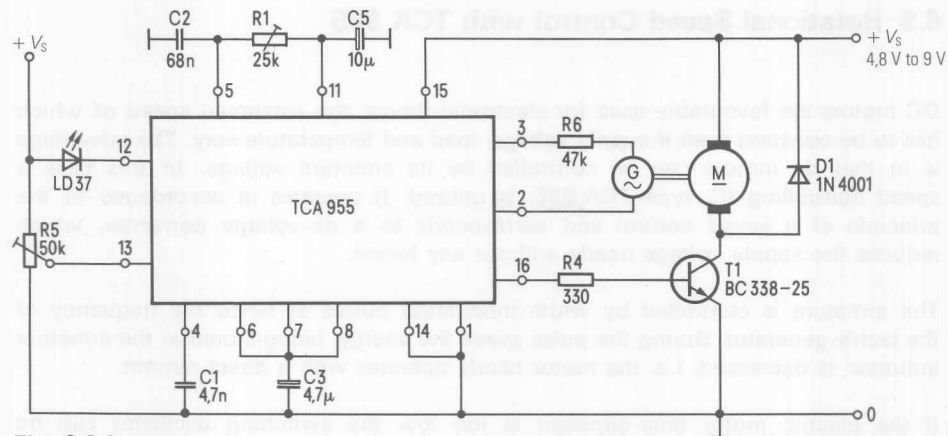


Fig. 6.9.1

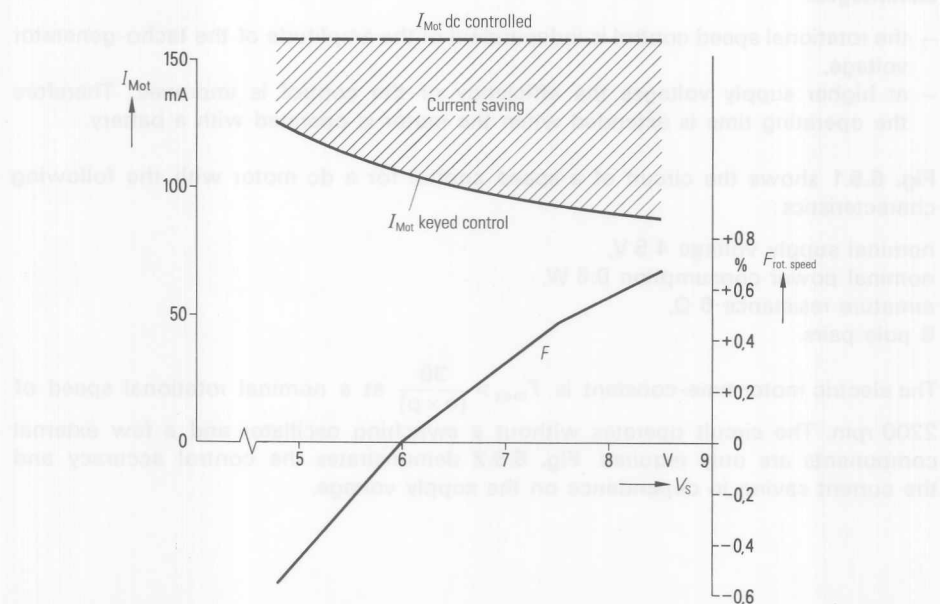


Fig. 6.9.2

Components for circuit 6.9.1

			Ordering code
1	Rotational speed control IC	TCA 955	Q67000-A983
1	Transistor	BC 338-25	Q62702-C314-V2
1	LED	LD 37 A	Q62703-Q99-S1
1	Diode	1N 4001	C66047-Z1306-A21
1	MKT-layer capacitor	4.7 nF/63 V	B32509-A472-M
1	MKC-layer capacitor	68 nF/100 V	B32540-C1683-J
1	Electrolytic capacitor	4.7 μ F/40 V	B41313-A7475-T
1	Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1	Resistor	330 Ω /0.5 W	B51261-Z4331-J1
1	Resistor	47 k Ω /0.5 W	B51261-Z4473-J1

6.10 Servo Control Using TCA 965 and DC Motor as Servo Actuator

In the following application the TCA 965 operates as a three-level controller. It continuously compares the value to be controlled (actual variable) with the desired one (reference variable) and generates a correcting signal for the manipulated variable. The circuit operates according to the principle of a follow-up control and it includes mechanical, electromechanical and electronic devices.

With an adequately-dimensioned servo control the dead zone, i.e. the error, is constant over the total control range. This constancy is also required for a hysteresis being eventually necessary. However, with servo control systems using the window discriminator TCA 965 these requirements are automatically guaranteed without great elaborateness of external components.

Fig. 6.10 shows the circuit of a servo control including the motor. The window is determined by the centre voltage V_8 and by a voltage V_9 corresponding to half of the window width. Actual and desired values are available as tapped voltages from the corresponding potentiometers, being both connected to voltage V_{10} . The potentiometer for the actual value is mechanically coupled to the motor. The dead zone is adjustable by potentiometer P_{dead} (twice V_9). A hysteresis possibly required is set by resistor R_H . The motor is part of a bridge circuit consisting of transistors T_1 to T_4 and being driven by the voltages of output 2 and 14 of the TCA 965. When the actual value $V_{6/7}$ is within the window, outputs 2 and 14 have the level of the supply voltage $+V_S$. In this case the motor stands still, i.e. it is short-circuited via T_1 and T_2 . When V_8 , for instance, varies towards the positive direction, i.e. setting of a new desired value, output 14 is connected to ground and output 2 is still on the level of supply voltage $+V_S$. Now T_1 and T_3 become conductive and T_2 and T_4 are cut off. The motor current flows in a direction where load and slider of the actual-value potentiometer are moved in that the same voltage as for the desired value is obtained.

As soon as the voltage $V_{6/7}$ for the actual value reaches the window edge, output 14 becomes $+V_S$ -level and the motor is again short-circuited via T_1 and T_2 . By the short-circuit procedure shorter break times are realized for the motor resulting in higher accuracy of the system.

The mechanical contacts connected to the INHIBIT-inputs have a stopper function, i.e. the motor is turned off when the given final position is reached. Instead of mechanical contacts contactless switches like Hall-ICs or proximity switches can also be used.

With the given constancy as well as the adjustment possibility for hysteresis and dead zone in the total control range every servo control can be optimized. That means an optimum with regard to accuracy, control time and stability can be realized under given conditions.

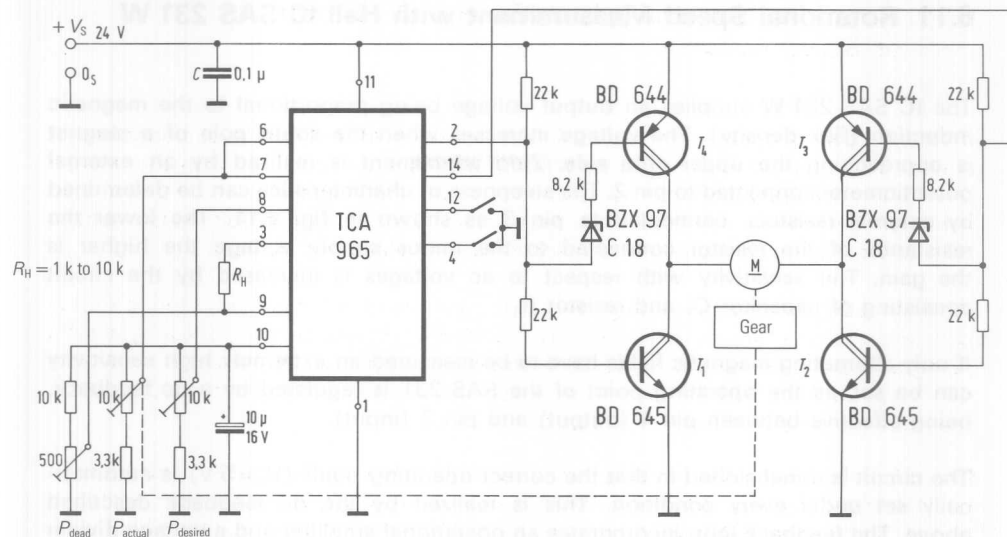


Fig. 6.10

Components for circuit 6.10

		Ordering code
1 Window discriminator IC	TCA 965	Q67000-A982
2 Darlington-Transistors	BD 644	Q62702-D230
2 Darlington-Transistors	BD 645	Q62702-D231
2 Z-diodes	BZX 97 C 18	Q62702-Z1241-F82
1 MKT-layer capacitor	0.1 μF/10 V	B32560-D1104-J
1 Electrolytic capacitor	10 μF/25 V	B41313-A5106-T
2 Resistors	3.3 kΩ/0.5 W	B51261-Z4332-J1
2 Resistors	8.2 kΩ/0.5 W	B51261-Z4822-J1
1 Resistor	10 kΩ/0.5 W	B51261-Z4103-J1
4 Resistors	22 kΩ/0.5 W	B51261-Z4223-J1

6.11 Rotational Speed Measurement with Hall IC SAS 231 W

The IC SAS 231 W supplies an output voltage being proportional to the magnetic induction (flux density). The voltage increases when the south pole of a magnet is approaching the upper chip side. Zero adjustment is realized by an external potentiometer connected to pin 2. The steepness of characteristics can be determined by external resistors, connected to pin 3 as shown in **fig. 6.11**. The lower the resistance of the resistor connected to the minus supply voltage the higher is the gain. The sensitivity with respect to ac voltages is increased by the circuit consisting of capacitor C_1 and resistor R_1 .

If only alternating magnetic fields have to be measured an extremely high sensitivity can be set, as the operating point of the SAS 231 is regulated by a dc feedback, being effective between pin 4 (output) and pin 2 (input).

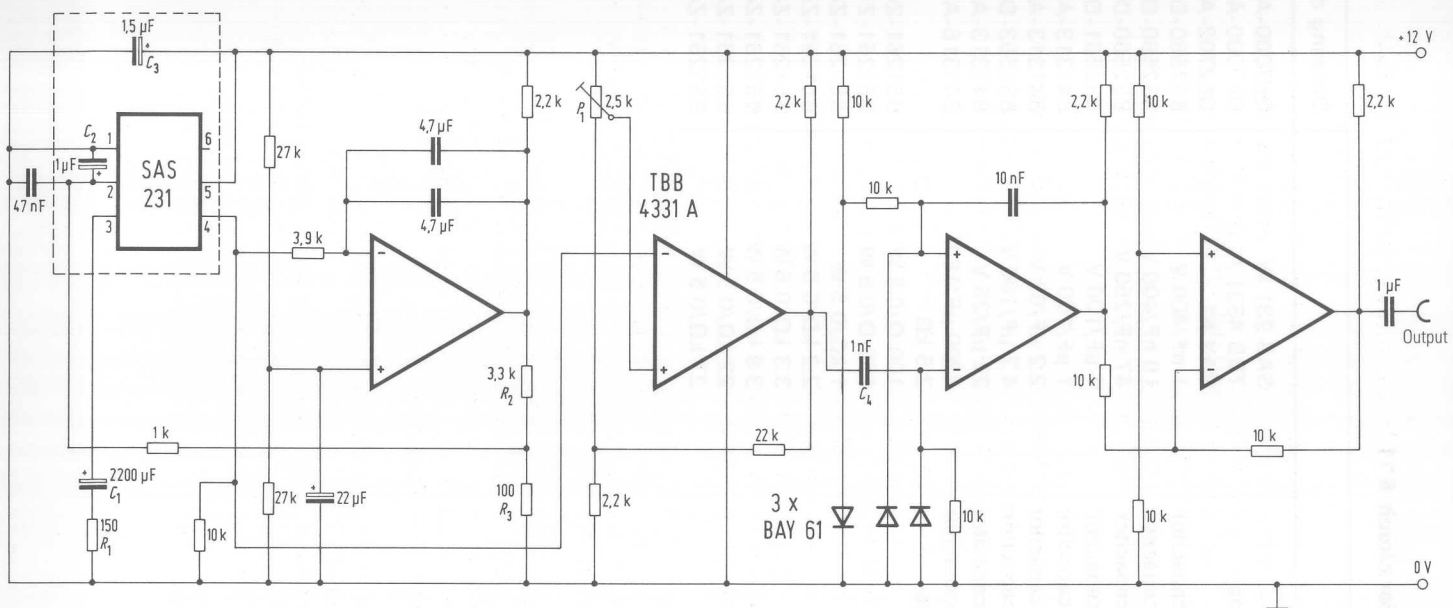
The circuit is dimensioned in that the correct operating point ($V_4 = 5\text{ V}$) is automatically set under every condition. This is realized by the dc feedback described above. The feedback loop incorporates an operational amplifier and a voltage divider (resistors R_2 and R_3). The divider ratio determines the setting of the operating point. Because of this strong dc feedback the temperature influence to the Hall IC is practically negligible. The capacitor C_2 has to be connected directly to pins 1 and 2 to avoid undesired influences of interferences. Besides that it is also convenient to place capacitor C_3 very close to the IC.

The output signal of the Hall-IC is supplied to another op amp operating as Schmitt-trigger to get a defined output signal even at small rotational speeds. The trigger threshold is adjustable by potentiometer P_1 . The Schmitt-trigger inverts the output signal of the SAS 231 W.

The following operational amplifier operates as monostable multivibrator. When an increasing voltage is applied via the capacitor C_4 to the inverting input (pin 10) a pulse with a width of approx. $70\text{ }\mu\text{s}$ is available at the output of this IC. This is always realized at the trailing edge of the SAS 231-output signal as it is inverted by the Schmitt-trigger.

An inverting buffer stage consisting of an op amp (no. 4) is connected to the monostable multivibrator. Thus short positive pulses with a constant duration are available at the output of the device, whereas a pulse corresponds to a rotation. The circuit shown in **fig. 6.11** is dimensioned in that the measuring range for rotational speeds covers 1 Hz to 10 kHz.

Fig. 6.11



Components for circuit 6.11

		Ordering code
1 Hall-IC	SAS 231 W	Q67000-A1468-W
1 Quad op amp	TBB 4331 A	Q67000-A1166
3 Diodes	BAY 61	Q62702-A389
1 MKT-layer capacitor	1 nF/400 V	B32560-D6102-J
1 MKT-layer capacitor	10 nF/400 V	B32560-D6103-J
1 MKT-layer capacitor	47 nF/250 V	B32560-D3473-J
1 MKT-layer capacitor	1 μ F/100 V	B32561-D1105-J
1 Electrolytic capacitor	1 μ F/100 V	B41313-A9105-T
1 Electrolytic capacitor	2.2 μ F/63 V	B41313-A8225-T
2 MKT-layer capacitors	4.7 μ F/100 V	B32563-D1475-M
1 Electrolytic capacitor	22 μ F/25 V	B41313-A5226-T
1 Electrolytic capacitor	2200 μ F/16 V	B41316-A4228-V
1 Potentiometer	2.5 k Ω	
1 Resistor	100 Ω /0.5 W	B51261-Z4101-J1
1 Resistor	150 Ω /0.5 W	B51261-Z4151-J1
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
5 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1 Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
1 Resistor	3.9 k Ω /0.5 W	B51261-Z4392-J1
1 Resistor	22 k Ω /0.5 W	B51261-Z4223-J1
2 Resistors	27 k Ω /0.5 W	B51261-Z4273-J1

6.12 Torque Measurement with Hall-Sensor

Torque measurement is based on determining the twist-angle which can be found out as follows. Two cams are placed on a shaft at a fixed axial distance. Now the shaft rotates and it is determined as to whether the two cams have the same position or not after a rotation. In the latter case this means that there is a twist angle, i.e. a torque. The difference in the positions can accurately be measured by using a Hall-sensor.

Fig. 6.12.2 shows a circuit for measuring the twist angle independent of the rotational speed. At the output of the two Hall-sensors sine-wave pulses are available (see fig. 6.12.1). They are generated when a cam passes the Hall-IC. These pulses are supplied to a Schmitt-trigger each (double operational amplifier-IC, type TBB 1458 B) and at its outputs two shifted rectangular pulses are available. The following EXOR-gates operate as buffer. The signal at its output is applied to another EXOR-gate, which supplies a signal when the two pulses of the Hall-sensor do not coincide. A following NAND-gate eliminates every second pulse originally caused by the coincidence of the trailing edges of the Hall-sensor signal. Thus a pulse, the length of which is directly proportional to the time shift of the sinus-wave signals, is generated. The following NAND-gate serves as buffer and its output signal as well as 1-MHz-pulses are processed by another NAND-gate, the output of which is also buffered by a NAND-gate.

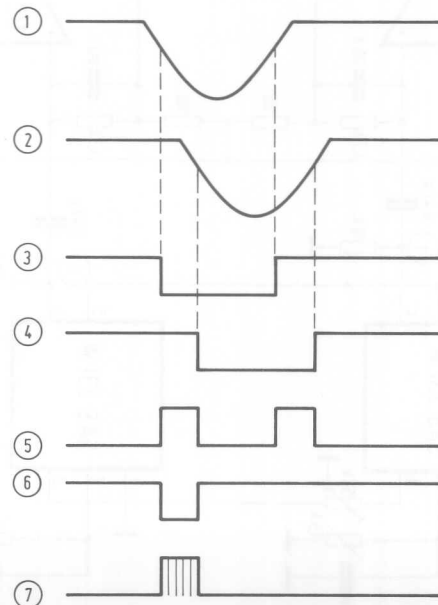


Fig. 6.12.1



to counter

If the number of 1-MHz-pulses is counted during a fixed reference time (e.g. 1 s), a quantity being proportional to the phase-angle is generated. It is independent of the rotational speed if the speed is not too low. A toothed wheel rim can be used to reduce the measuring time, that means to increase the accuracy. In this case, however, an extreme accuracy of all mechanical parts is required.

Components for circuit 6.12

		Ordering code
1 Hall-IC	SAS 231 W	Q67000-A1468W
1 Double op amp	TBB 1458 B	Q67000-A1036
4 NAND-gates	4010	—
3 EXOR-gates	4030	—
1 Z-diode	BZX 97/C5V6	Q62702-Z1229-F82
2 MKH-layer capacitors	100 nF/100 V	B32510-D1104-K
2 MKM-layer capacitors	220 nF/100 V	B32511-D1224-K
2 MKM-layer capacitors	0.47 μ F/100 V	B32512-D1474-K
2 Electrolytic capacitors	100 μ F/16 V	B41283-B4107-T
1 Potentiometer	50 k Ω	—
2 Resistors	100 Ω /0.5 W	B51261-Z4101-J1
3 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
2 Resistors	10 k Ω /0.5 W	B51261-Z4103-J1

6.13 Interference-Immune Timing Circuit with FZK 101

The timing IC FZK101 operating as monostable multivibrator has to be mounted on a pc board according to RF requirements to take full advantage of interference immunity for the Siemens low-speed logic (LSL-family). As shown in **fig. 6.13** the pc board should be copper-faced around the IC as much as possible. The supply voltage is applied to pin 16 via a 100 nF-capacitor specified for RF-signals. The lines for input and output have to be screened. Besides that pins 5, 11, 12 and 13 have to be connected to ground via 1 nF-capacitors. But it has to be considered that these capacitors generate an additional time delay for the output pulse edge.

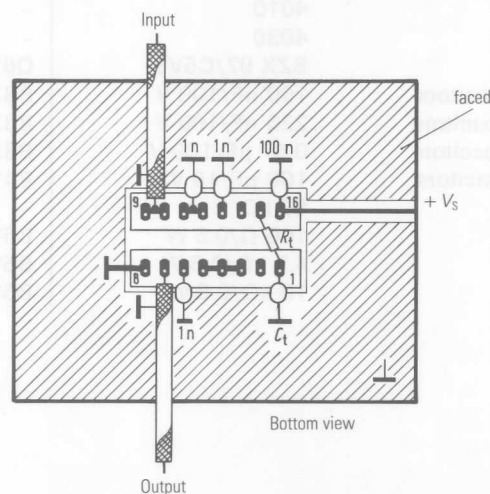


Fig. 6.13

Components for circuit 6.13

		Ordering code
1 LSL-timing circuit	FZK 101	Q67000-K6
3 Ceramic capacitors	1 nF/25 V	B37982-S0102-M3
1 Ceramic capacitor	100 nF/32 V	B37463-A3104-S
1 MKT-layer capacitor or Polypropylene capacitor	Capacitance depends on pulse width	—
1 Resistor	Resistance depends on pulse width	—

7. Circuits for Electric Power Engineering

7.1 Electronic Dimmer Using S 576

The MOS dimmer S 576 is an advanced type of the well-known IC S 566. It comprises a trigger circuit for a triac in that the driver transistor is no longer necessary. Pin 2 is the dimmer input of the S 576. When this function is not required a reference level of 0 V ($\cong$ phase) has to be applied to this input. Compared to previous solutions the capacitor connected originally to pin 2 is no longer necessary.

Operation principle of the MOS-dimmer IC

The operation principle of a touch sensor is in that the resistance between human body and ground is finite. Therefore the input level of any electronic circuit can be influenced, i.e. switches or control functions can be realized. As with a sensor only the instructions "on", "off" and "phase angle variation" have to be controlled, the time of touching the sensor is the only criterion. Processing and storing of this information as well as triggering the triac is realized by the integrated MOS circuit S 576. Internal clock and synchronisation with frequency and phase of the mains is generated by a phase locked loop circuit (PLL). Because of its digital operation every required phase angle is accurately and constantly adjusted. The triac is fired every half-wave by a pulse with a duration of approx. 30 μ s being supplied to pin 8.

Application

Fig. 7.1.1 shows a dimmer circuit for incandescent lamps. It replaces the conventional mechanical switch contact being in series to the lamp. In this case the function of the contact is realized by the triac. When it is turned off the total supply voltage is applied to the triac. During the conductive state the residual voltage only drops across the triac.

But this electronic control circuit requires a supply voltage of 15 Vdc. Therefore the S 576 is dimensioned in that a phase angle minimum of approx. 30° can be adjusted. The voltage being available during this angle is rectified by D_2 and it charges capacitor C_3 to the supply voltage of the IC. As the supply current is very low an electrolytic capacitor with a small capacitance can be used. The current of z-diode D_1 is limited by R_1 and C_2 . Radio interferences are eliminated by capacitor C_1 and choke Ch.

The synchronisation to mains frequency is obtained by the ac voltage which is supplied from A_2 of the triac to pin 4 of the IC via resistor R_2 . C_4 suppresses interference signals probably imposed. Capacitor C_5 is part of the internal control circuit of the S 576. When the sensor is touched the level of the voltage divider, connected to the control input (pin 5) is influenced. R_8 and R_9 are necessary as protection resistors against electric shock hazards. The sensitivity of the sensor is adjusted by R_7 . Additional touch sensors cannot be connected in parallel, as the circuit has a highly resistive termination and therefore it is very sensitive against

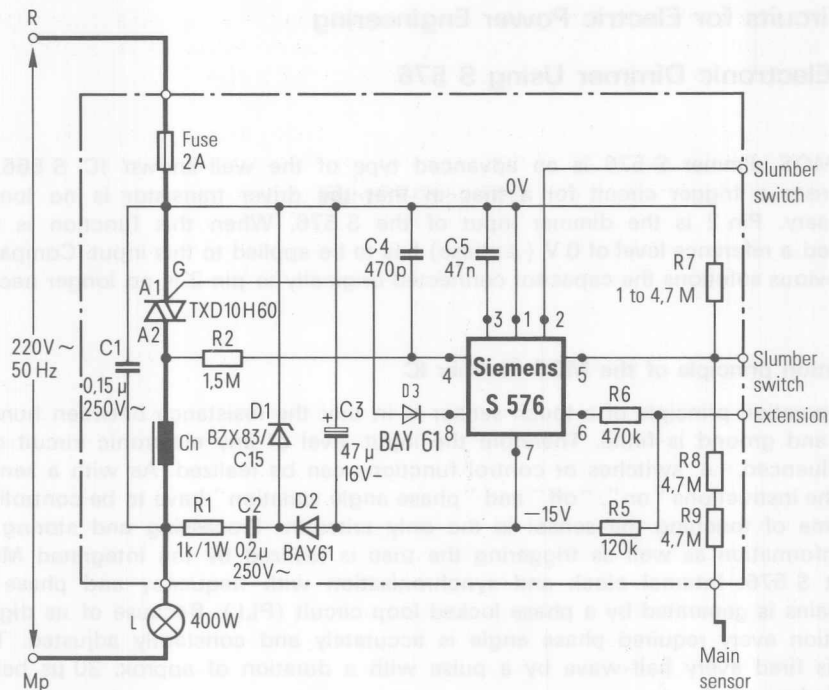
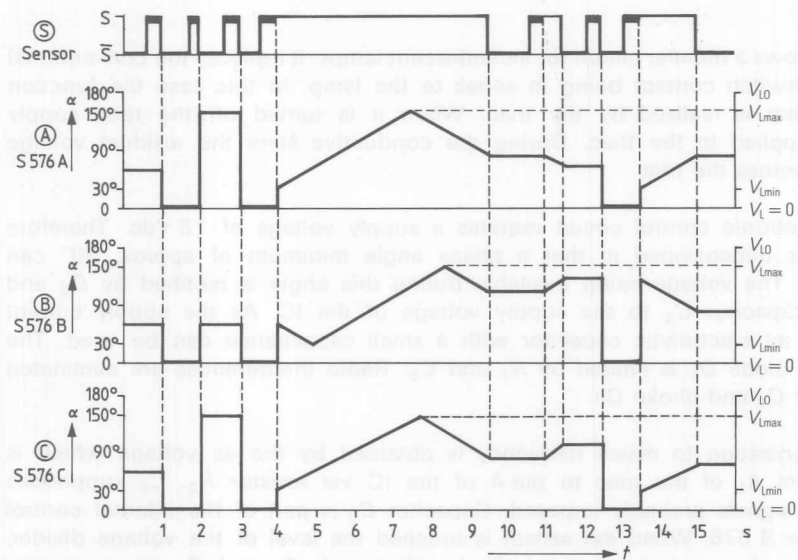


Fig. 7.1.1



α Angle of current flow
 V_L Lamp voltage
 S Control signal: S Sensor touched
 ($\blacksquare$ < 0.4 s, $\rightarrow$ 0.4 s)
 $\bar{S}$ Sensor not touched

Fig. 7.1.2

interference signals which may be picked up by long lines. In this case another inverted input, which can be terminated with a lower resistance is provided for. For controlling this input an extension circuit is shown in **fig. 7.2.1**.

Resistors R_5 and R_6 limit the current in case that a wrong polarity is applied to the extension input. If no additional sensor is required these two resistors are not necessary. In this case pin 6 has to be connected to pin 7 (V_{DD}).

For an accurate operation of the sensor it is necessary that voltages with correct polarity are applied to the IC, i.e. the phase has to be supplied to R and L has to be connected to ground Mp via lamp.

The triac operates in the 3rd and 4th quadrant of the I-U-characteristics. Diode D_3 limits voltage peaks, sometimes generated at the gate of T_c , to a value of less than $V_{ss} + 0.5V$ (pls. refer to characteristics). Diode D_3 is not required if suitable triacs are used. This special feature of the triac depends on anode current and on internal impedance between G and A_1 . It can be measured and specified by the manufacturer. The admissible power dissipation of the load is limited by the maximum ratings of selected triac. The RFI suppression circuit has to be correspondingly dimensioned. The surge current generated during turn-on of the incandescent lamp due to a very low cold resistance has to be considered. It can exceed 5 to 10 times the nominal lamp-current.

Control behaviour

The three types S 576 A, B and C differ in their control behaviour as follows:

- S 576 A: At turn-on the brightness maximum is always set. During dimming the operation starts from brightness minimum. If a dimming is repeated the control is attained in the same direction, e.g. brighter.
- S 576 B: At turn-off the selected brightness is correspondingly stored and set again when the device is turned on. During dimming the control operation starts from this stored brightness value. If the dimming is repeated the direction of control is reversed.
- S 576 C: At turn-on the brightness maximum is always set. During dimming the operation starts from brightness minimum. If the dimming is repeated the direction of control is reversed.

Fig. 7.1.2 demonstrates the described control behaviour. At beginning the dimmer is turned off by a short touch of the sensor.

On/off-switch S 576 D

When the sensor area is touched for more than 50 ms a lamp is alternatively turned on at brightness maximum or switched off. The switching operation is released at the beginning of the touch.

Turn-off and downward dimming of the lamp is possible via clock input 2 as featured by the other brightness control devices.

Components for circuit 7.1.1

		Ordering code
1	Electronic dimmer S 576	Q67100-Y506
1	Triac TXD 10 H60	C67048-A1505-A6
1	Z-diode BZX 83/C15	Q62702-Z1081-F82
1	Si-switching-diode BAY 61	Q62702-A389
1	Ceramic-disc capacitor SDPN, 470 pF/400 V	B37205-A5471-S1
1	MKT-layer capacitor 47 nF, 250 V, $\pm 5\%$	B32560-D3473-J
1	RFI suppression capacitor 0.15 μ F, 250 V	B81111-B-B27
1	RFI suppression capacitor 0.2 μ F, 250 V	B81111-B-B28
1	Al-electrolytic capacitor 47 μ F, 16 V	B41316-A4476-V
4	Carbon layer resistors 1 to 4.7 M Ω , 0.5 W, $\pm 5\%$	B51261-Z4...-J1
2	Carbon layer resistors 4.7 M Ω /0.5 W, $\pm 5\%$ high-tension proof	
1	Carbon layer resistor 1 k Ω , 1 W	B51276-A2102-G
1	RFI suppression choke	B82603-V-B11
1	Fuse 2 A, medium-acting	—

7.2 Extension for Dimmer ICs S 566 and S 576

As against IC S 566 the advanced type S 576 requires a modified circuit for the electronic extension to guarantee a higher interference immunity. The following describes an extension circuit which is compatible with both types, S 566 and S 576.

The integrated circuits S 566 and S 576 had been designed for operation with several extensions, i.e. the device replacing conventional double-throw and intermediate switches can be operated by parallelly arranged sensors. These extensions can be realized by mechanical push buttons or by suitable electronic circuits with touch sensors.

The advanced devices of the S 576-family operate with a modified logic for the extensions. During both mains half-waves an H-level has to be applied to the input to release a switching. Thus ac voltages cannot interfere. But this operation requires a modified circuit for the electronic sensor extension. **Fig. 7.2.1** shows a recommended circuit. During the negative half-wave the H-level is maintained by a reset delay. When the sensor is touched both transistors T_1 and T_2 have to be conductive. During the positive half-wave C_1 is charged to a z-voltage of 6.8 V. During the negative half-wave capacitor C_1 supplies the base current for transistor T_2 . The circuit is dimensioned in that ac currents coupled in via the line capacitor C_{line} will not generate an extension voltage higher than 1.5 V, when T_1 and T_2 are conductive (H-level).

The response time is approx. 2 ms and the reset delay amounts approx. 30 ms. The sensitivity maximum of the sensor is at approx. 50 pF.

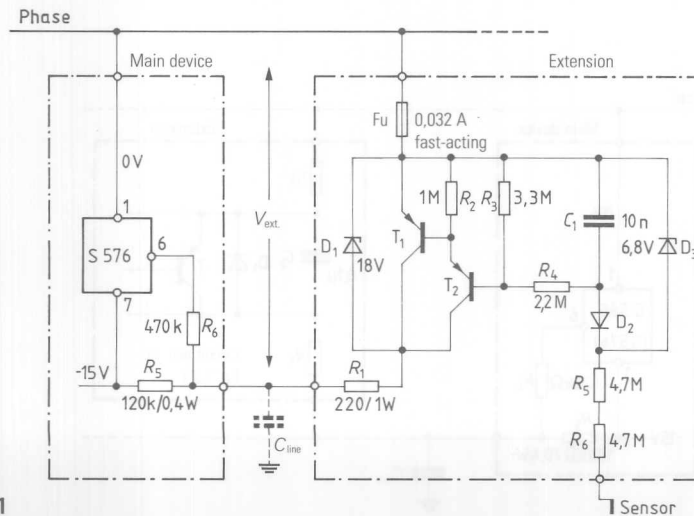


Fig. 7.2.1

Compatibility of the extension with S 566 and S 576

Both types S 566 and S 576 can be operated by extensions with mechanical keys or with electronic circuits accordingly to fig. 7.2.1. For S 566 an attenuation of the coupled-in interference voltage is recommended in any case. Thus an undesired turn-on is prevented even at line capacitances being greater than approx. 1 nF. Basically there are two possibilities for the attenuation:

- The compensation capacitor is located in the main device (see **fig. 7.2.2**).
 Advantage: as many extensions as required can be connected.
 Disadvantage: space requirement in the main device.
- The compensation capacitor is located in the extension circuit as shown in **fig. 7.2.3**.
 Advantage: no problems regarding space.
 Disadvantage: limited number of extensions (max. 3).

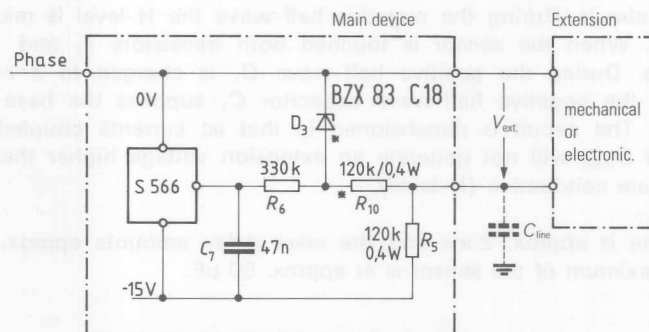


Fig. 7.2.2

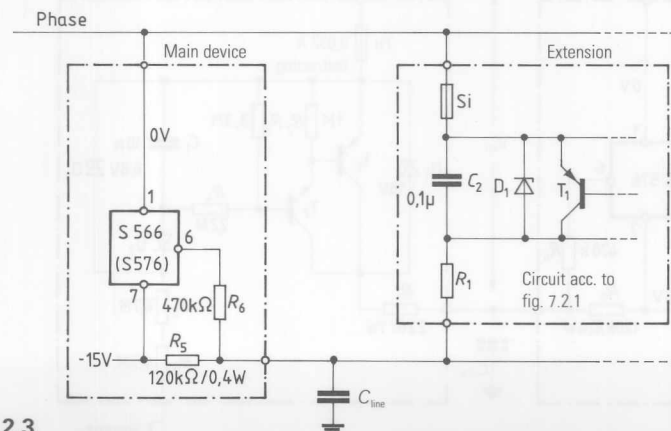


Fig. 7.2.3

Possibility a (fig. 7.2.2)

Z-diode D_3 limits the amplitude of superimposed signals if the extension circuit operates with mechanical push buttons. Series resistor R_{10} protects diode D_3 in the case of incorrect polarization of the applied voltages. These two components are not necessary if an electronic extension according to fig. 7.2.1 is used. If there exists an imposed ac voltage capacitor C_7 is charged to a dc-level of approx. $0.5 \times V_z \approx 9 \text{ V}$ (D_3), being superimposed by a triangular voltage. The amplitude of the extension circuit voltage is -6.5 V max. at $C_{\text{line}} = 17 \text{ nF}$ and $C_7 = 47 \text{ nF}$. Thus it is lower than the threshold minimum of -5 V . This value corresponds to practical results with components from mass production. It is higher than the standard one specified in the data sheet with $V_{\text{IL}} = -8 \text{ V}$.

Should the production of dimmers probably be switched to main devices with S 576, the high interference immunity can be advantageously utilized without modifying the extensions.

Possibility b (fig. 7.2.3)

With this circuit the capacitances of all compensation capacitors are added. At mains failure these capacitors have to be charged within the immunity time of the input, otherwise an H-level signal will be recognized. Therefore the total capacitance is limited and its permissible maximum is approx. 400 nF with reference to circuit 7.2.3 and with $R_5 = 120 \text{ k}\Omega$. With a compensation capacitance of 100 nF for each extension, up to 3 extensions can be connected to the mains device. This fact generally represents a compromise between sufficient interference immunity and number of possible extensions for all practical applications. Thus an earth capacitance of approx. 3 nF can be compensated per extension.

Should the production switch to a device with S 576 the extensions can be used without any modifications. Up to 3 extensions can only be connected with utilizing the total interference immunity if extensions without capacitors are used (time constant!).

2 Transistors	BC 308 B	Q62702-C286
1 Z-diode	BZX 97/C6V8	Q62702-Z1231-F82
1 Z-diode	BZY 97/C18	Q68000-A959-F82
1 Diode	BAY 61	Q62702-A389
1 MKT-layer capacitor	10 nF/100 V	B32510-D1104-K
1 Resistor	220 Ω /1 W	B51276-A2221-G
1 Resistor	2.2 M Ω /0.5 W	B51261-Z4125-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1
1 Resistor	3.3 M Ω /0.5 W	B51261-Z4335-J1
2 Resistors	4.7 M Ω /0.5 W	

Components for circuit 7.2.2

1 Z-diode	BZX 83 C 18	Q62702-Z1083-F82
1 MKT-layer capacitor	47 nF/100 V	B32510-D1104-K
2 Resistors	120 k Ω /0.5 W	B51261-Z4124-J1
1 Resistor	330 k Ω /0.5 W	B51261-Z4334-J1

Components for circuit 7.2.3

1 MKT-layer capacitor	0.1 μ F/100 V	B32510-D1104-K
1 Resistor	120 k Ω /0.5 W	B51261-Z4124-J1
1 Resistor	470 k Ω /0.5 W	B51261-Z4474-J1

7.3 Slumber Switch with S 576

The IC S 576 features the functions on/off-switching and dimming a lamp by means of a main control or by several extensions. Besides that it offers the possibility to realize a so-called slumber switch in conjunction with an external clock generator.

A slumber switch is characterized in that after operating, the light is continuously reduced to a minimum within a given time and then completely turned off. The dimming-down time of the circuit shown in **fig. 7.3** is adjustable between 10 and 60 min. The number of components required for the slumber switch is kept to a minimum to place the circuit and the main control unit (MOS-dimmer S 576, triac etc.) in a buried wall box (55 mm). The slumber switch can be operated by a second sensor area or by push button T.

The supply current of this additional circuit is less than 100 μA as a logic CMOS IC is used.

Fig. 7.3 shows the circuit of the slumber switch. It includes the main control unit with S 576 and the additional circuit with a flip-flop, two CMOS-NAND gates G_1 and G_2 and an RC clock generator.

IC S 576 operates digitally. Every clock pulse at pin 2 influences insignificantly the phase control angle of the triac in that the brightness is almost innoticeably reduced. The lamp is turned off at the 84th pulse.

When the sensor area of the slumber switch is touched the monostable multivibrator flips. Output of gate G_1 shows an H-level and enables the clock generator, the output pulses of which are supplied to S 576. The clock generator operates as long as the sensor of the main control unit is touched again. In this case the output at gate G_2 gets an H-level and the monostable multivibrator flips back and stops the clock generator.

The clock generator comprises gate G_3 and two transistors T_1 and T_2 . The push-pull output of G_3 applies alternatively a voltage of 0 V or -15 V to resistors R_4 and R of the time-determining RC-circuit. The emitter voltage of T_1 is switched between -4.5 and -10.5 V via resistor R_4 . The voltage at capacitor C_2 follows the level at the emitter and causes the flipping of gate G_3 when T_2 has reached its switching point.

The repetition period T_{clock} of the clock pulses depends on the time constant of the RC-circuit and on the voltage variation at the emitter of T_2 . In the described circuit the repetition period is calculated as follows:

$$T_{\text{clock}} = 1.79 \times R \times C_2.$$

The period is adjustable from 8.4 to 44.2 s by potentiometer R_5 . The dimming-down interval is then 12 to 62 min.

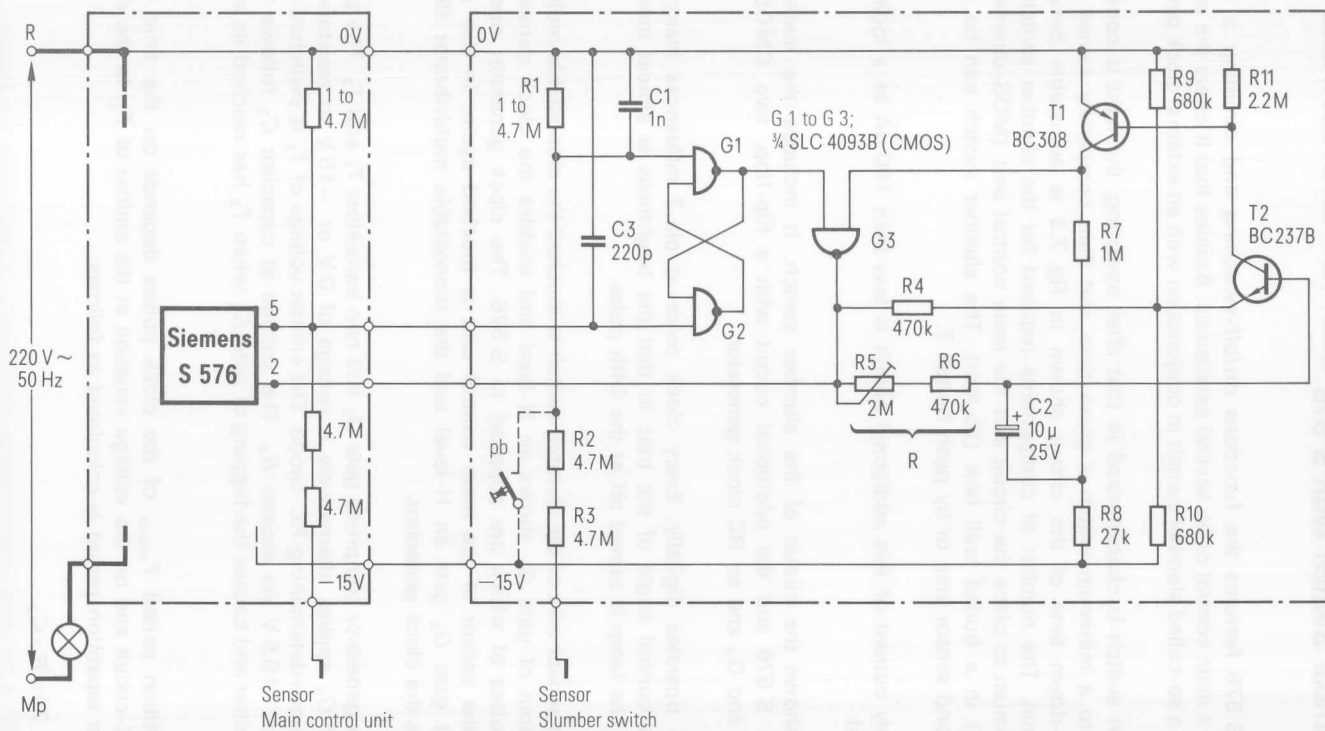


Fig. 7.3

Slow edges of the switching pulses cause relatively high supply currents of 1.5 mA at the CMOS gates. Therefore a steep slope for the input pulse at gate G_3 is generated by transistors T_1 and T_2 . By this measure the total supply current of the circuit can be reduced to a value between 25 and 100 μ A.

Components for circuit 7.3

		Ordering code
1 CMOS-NAND-Schmitt-trigger	SLC 4093B	—
1 Silicon-PNP-transistor	BC 308	Q62702-C704
1 Silicon-NPN-transistor	BC 237B	Q62702-C277
1 Ceramic-disc capacitor	220 pF, 400 V	B37205-A5221-S1
1 MKT-layer capacitor	1 nF, 400 V	B32510-D6102-K
1 Tantalum capacitor	10 μ F, 25 V	B45181-B3106-M
8 Carbon layer resistors	1 to 4.7 M Ω , 0.5 W	B51261-Z4...-J1
2 Carbon layer resistors	4.7 M Ω /0.5 W, $\pm$ 5% high-tension proof	
1 Potentiometer	2 M Ω , 0.1 W	—

7.4 Sensor Dimmer for Single- and Double-Phase Operation

The Siemens IC-family of MOS-dimmers is dimensioned for operation with one phase and ground (Mp). The sensor is scanned at approx. 20° after the zero-axis crossing of the phase voltage.

In foreign countries the dimmer very often has to operate with the two phases of a three-phase supply network. In this case the phase difference between sync and sensor signal is too great. The dimmer IC cannot be controlled.

However, with the circuit shown in **fig. 7.4** the operation of the sensor dimmer does not depend on the phase relationship. During both mains half-waves an H-level is applied to the extension input of the dimmer IC. This dc voltage control is realized by capacitor C_1 . It keeps transistor T_1 conductive during the negative mains half-wave.

With an H-level of ≥ -2 V the circuit operates with S 566 as well as with S 576.

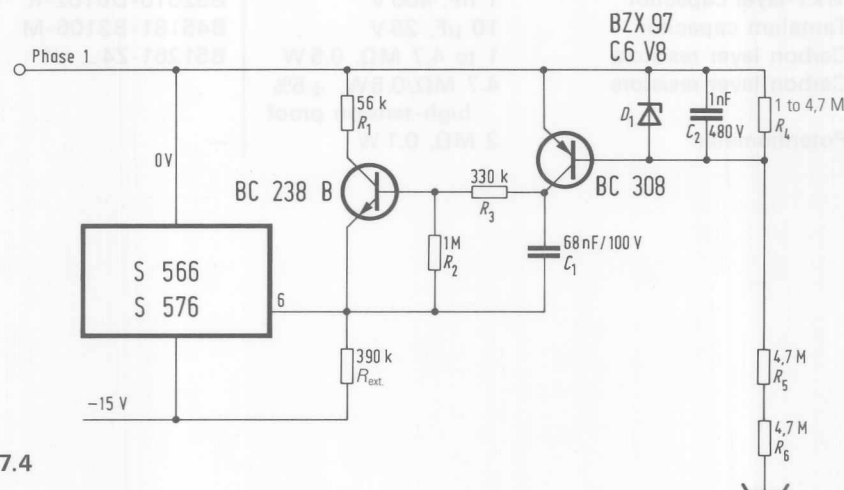


Fig. 7.4

Components for circuit 7.4

		Ordering code
1 Transistor	BC 238 B	Q62702-C279
1 Transistor	BC 308	Q62702-C704
1 Diode	BAY 61	Q62702-A389
1 MKT-layer capacitor	1 nF/400 V	B32510-D6102-K
1 MKT-layer capacitor	68 nF/100 V	B32510-D1683-K
1 Resistor	56 kΩ/0.5 W	B51261-Z4563-J1
1 Resistor	330 kΩ/0.5 W	B51261-Z4334-J1
1 Resistor	1 MΩ/0.5 W	B51261-Z4105-J1
2 Resistors	4.7 MΩ/0.5 W	B51261-Z4475-J1
high-tension proof		
1 Resistor	1 to 4.7 MΩ/0.5 W	B51261-Z4...-J1

7.5 Excess Temperature Protection for Dimmer IC S 576

As shown in **fig. 7.5** a PTC resistor is utilized to protect the dimmer IC against inadmissible excess temperatures during operation. When the PTC resistor is heated up its resistance is high and the firing current of the triac is decreased in that the triac is turned-off. After a cooling period the device is automatically switched on again. The triac turn-off has the advantage against switching off the supply voltage for the total circuit in that the IC operates completely and offers all functions. Therefore after cooling-off the brightness corresponds to the previously set value again.

The IC is protected by a PTC resistor, type P 350-B 11. It is connected between pin 8 of the S 576 and the gate of the triac. Its reference temperature is 80 °C. According to the data sheet this PTC resistor has a resistance of up to 200 Ω. Therefore it is only applicable for triacs with a trigger current of ≤ 50 mA. For other reference temperatures corresponding types of PTC resistors have to be used.

Components for circuit 7.5

		Ordering code
1 PTC-resistor	P 350-B 11	Q63100-P350-B11

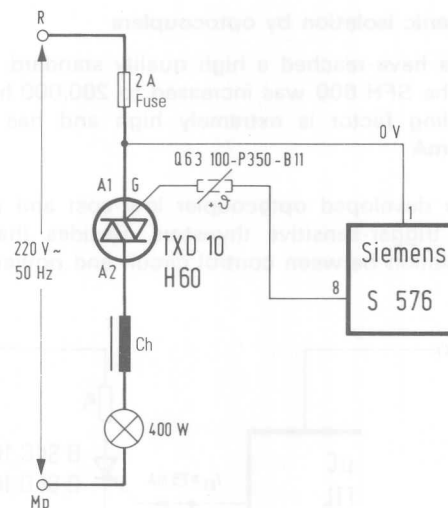


Fig. 7.5

7.6 Low-Cost Control Circuit for Trigger-Sensitive-Thyristors and Triacs

The new designed trigger-sensitive thyristors of type series BSt C10 and BSt D10 require only approx. 5 to 10% of the firing current which is needed for standard types.

The trigger-sensitive triacs TXC 10 and TXD 10, trigger class H, have a sensitivity which is twice the one of other conventional types.

Therefore these modern power semiconductors can be controlled by simple circuits reducing system costs.

Thyristors and triacs can be triggered by short pulses with $t \leq 100 \mu\text{s}$, by long pulses with $t \leq 1 \text{ ms}$ and by permanent pulses. Thyristors can only be fired when a positive half-wave voltage is applied to the anode.

Direct thyristor triggering

I/O-interface ICs of microcomputer systems, TTL circuits or MOS logic ICs supply an output current of approx. 10 mA at H-level (see **fig. 7.6.1**). This current is sufficient for firing trigger-sensitive thyristors with a trigger current maximum of $I_{GT\text{max}} \leq 5 \text{ mA}$. The negative temperature coefficient of the trigger current causes an increase to $I_{GT} \approx 7.5 \text{ mA}$ at $T_{\text{amb}} = -20^\circ\text{C}$. The L-level has to be less than 0.2 V to turn off the thyristor safely. It is, however, further reduced by $R_1 \approx 4.7 \text{ k}\Omega$.

Triggering with galvanic isolation by optocouplers

Modern optocouplers have reached a high quality standard. By new technologies the half-life time of the SFH 600 was increased to 200,000 h. The isolation voltage is 2.5 kV, the coupling factor is extremely high and has a value between 63 and 500% at $I_F = 10 \text{ mA}$.

Because of this new developed optocoupler low-cost and reliable trigger circuits can be realized for trigger-sensitive thyristors. Besides that they offer also the required galvanic isolation between control circuit and power stage.

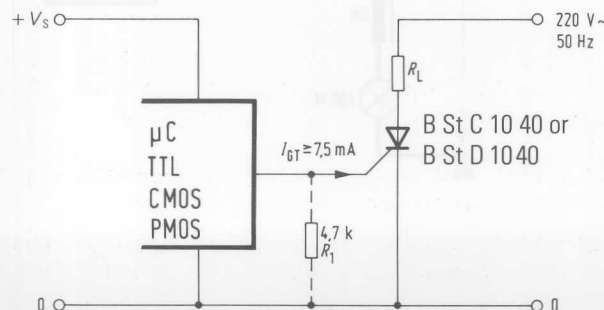


Fig. 7.6.1

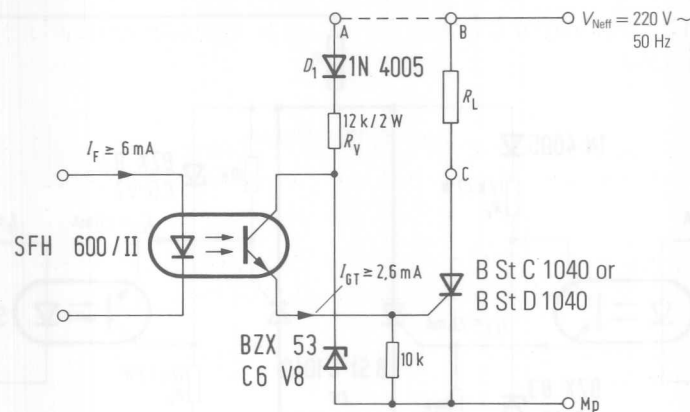


Fig. 7.6.2

Half-wave control

In the circuit of **fig. 7.6.2** the trigger current is supplied from the mains via series resistor R_V . The circuit has to be dimensioned in that a power minimum is dissipated in R_V and a wide range of current-flow angle is realized. It is reduced to 50% by diode D_1 . A z-diode limits the reverse voltage at the collector of the phototransistor.

If a connection is made from A to C (instead of B) the power dissipation of R_V is reduced when the thyristor is fired. Disadvantageous effects can be caused by the basic current of the resistive load when the thyristor is turned off.

Full wave control

Fig. 7.6.3 shows the control of an antiparallel thyristor circuit. This circuit and the one shown in **fig. 7.6.2** operate in a trigger range between 6 and 174° . Short, long and permanent pulses are possible for the triggering.

Trigger current supply with series resistor and capacitor, control range $\varphi = 0$ to 180° (short, long and permanent pulses).

Capacitor C_S stores the required trigger energy during the negative half wave of the mains voltage. Therefore the phase angle is between 0 and 180° (see **fig. 7.6.4**).

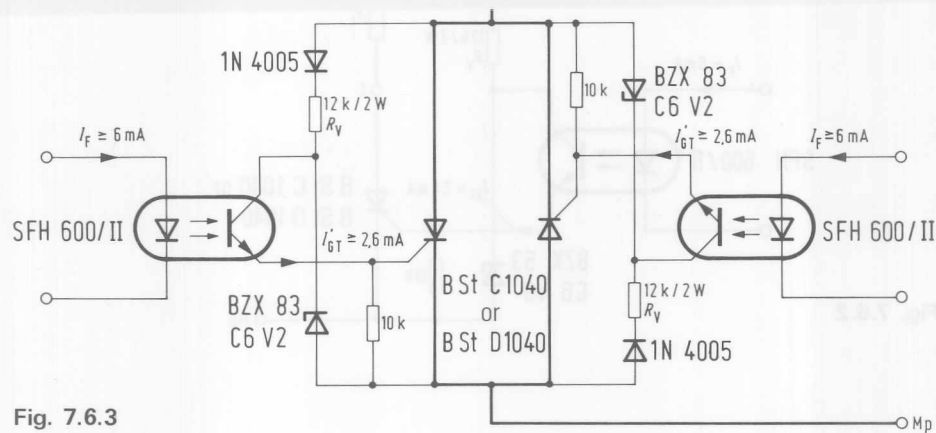


Fig. 7.6.3

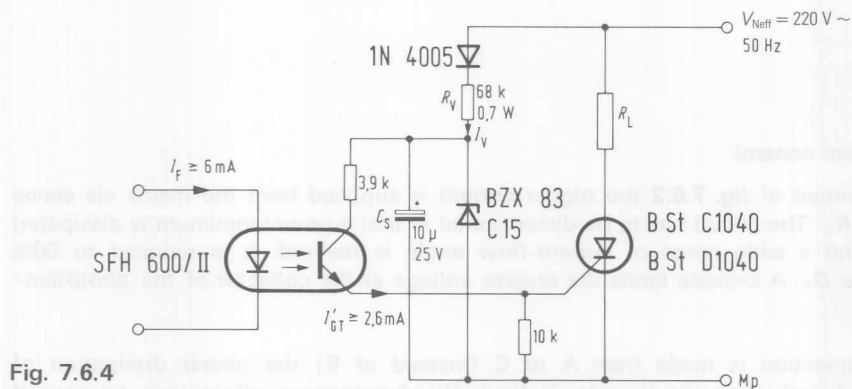
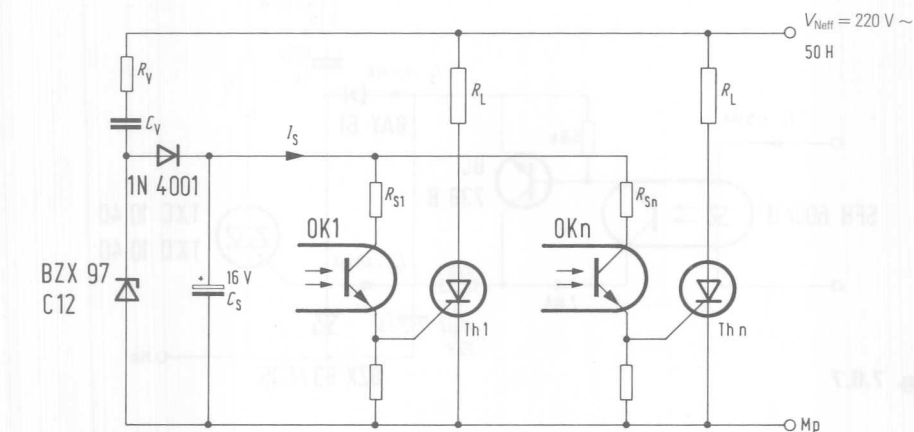
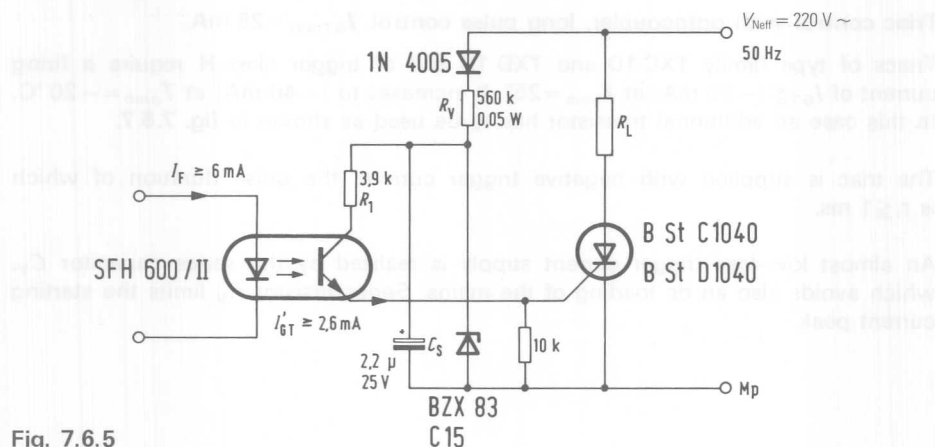


Fig. 7.6.4

Trigger current supply with series resistor and capacitor, control range $\varphi=0$ to 180° (long pulses).

The power dissipation of R_V and C_S can essentially be reduced if the optocoupler is operated by trigger pulses with $t_i \leq 1$ s (see fig. 7.6.5).

Thyristors with higher trigger currents require a proportional capacitance increase of C_S and an indirect proportional resistance reduction of R_V and R_1 .



Common trigger current supply for several trigger-sensitive thyristors with series capacitor.

For triggering several thyristors a low-loss power supply with series capacitor is recommended. The circuit is shown in **fig. 7.6.6**. The capacitance of C_V determines the available maximum of current I_S . It is

$$I_S \approx 2.82 \times C_V \times V_{Neff} \times f.$$

Series resistor R_V limits the starting current peak.

With $C_V = 0.68 \mu F$ the available current maximum is $I_S = 21$ mA. In this case 15 thyristors of class H can be triggered by permanent pulses with a duration of 10 ms.

Triac control with optocoupler, long pulse control, $I_{GTmax} = 25 \text{ mA}$

Triacs of type family TXC 10 and TXD 10 and of trigger class H require a firing current of $I_{GT} \leq |-25 \text{ mA}|$ at $T_{amb} = 25^\circ$. It increases to $|-40 \text{ mA}|$ at $T_{amb} = -20^\circ \text{C}$. In this case an additional transistor has to be used as shown in fig. 7.6.7.

The triac is supplied with negative trigger current, the pulse duration of which is $t_i \leq 1 \text{ ms}$.

An almost low-loss trigger current supply is realized by the series capacitor C_V , which avoids also an dc loading of the mains. Series resistor R_V limits the starting current peak.

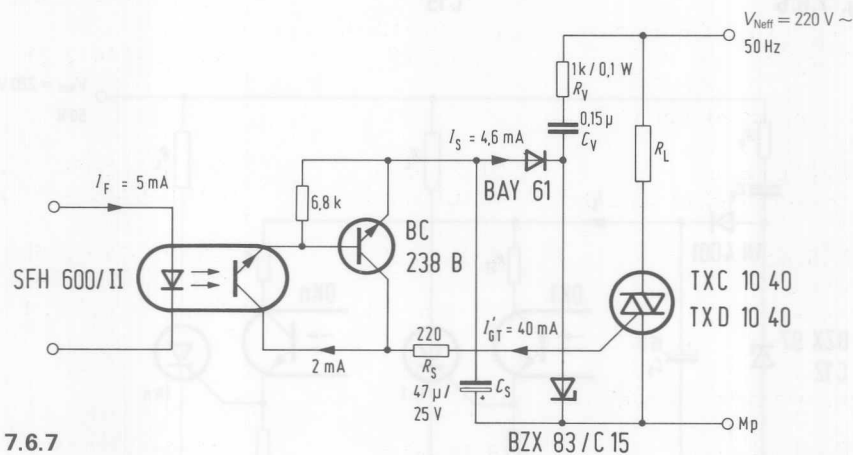


Fig. 7.6.7

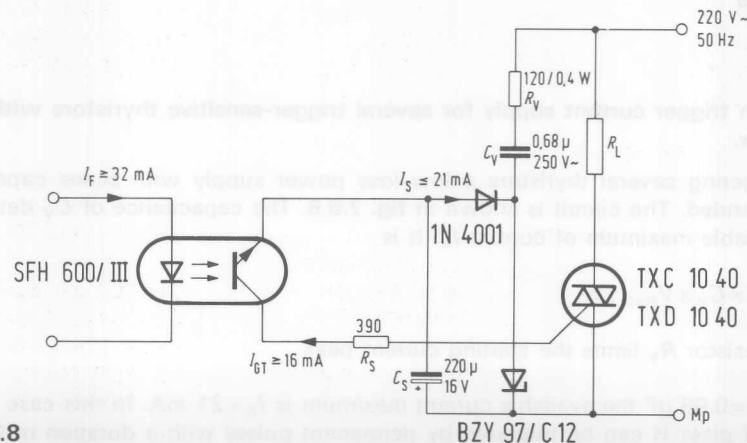


Fig. 7.6.8

Trigger control with permanent pulses, $I_{GTmax} \leq 10 \text{ mA}$

Triacs of the same type family with still higher trigger-sensitivity ($I_{GTmax} \leq 10 \text{ mA}$) can be directly fired by the phototransistor of the optocoupler.

Fig. 7.6.8 demonstrates a trigger circuit for permanent pulses. For long pulse triggering (i.e. $I_{GT} \leq 10 \text{ mA}$) components C_V , C_S and R_V have to be correspondingly dimensioned as shown in the components list.

Components for circuit 7.6.1

		Ordering code
1 Thyristor, trigger class S1, S2 or D	BStC1040 (or BStD1040)	C67048-A1425-A29
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1

Components for circuit 7.6.2

1 Opto coupler	SFH 600/II	Q68000-A5054
1 Thyristor, trigger class S2	BStC1040 (or BStD1040)	C67048-A1425-A29
1 Z-diode	BZN 83/C6V8	Q62702-Z1073-F82
1 Diode	1N4005	C66047-Z1306-A25
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	12 k Ω /2 W	—

Components for circuit 7.6.3

2 Opto couplers	SFH 600/II	Q68000-A5054
2 Thyristors, trigger class S2	BStC1040 (or BStD1040)	C67048-A1425-A29
2 Z-diodes	BZX 83/C6V2	Q62702-Z1072-F82
2 Diodes	1N4005	C66047-Z1306-A25
2 Resistors	10 k Ω /0.5 W	B51261-Z4103-J1
2 Resistors	12 k Ω /2 W	—

Components for circuit 7.6.4

1 Opto coupler	SFH 600/II	Q6800-A5054
1 Thyristor, trigger class S2	BStC1040 (or BStD1040)	C67048-A1425-A29
1 Z-diode	BZX 83/C15	Q62702-Z1081-F82
1 Diode	1N4005	C66047-Z1306-A25
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Resistor	3.9 k Ω /0.5 W	B51261-Z4392-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	68 k Ω /1 W	B54313-Z5683-G1

Components for circuit 7.6.5

		Ordering code
1	Opto coupler	SFH 600/II
1	Thyristor, trigger class S2	BStC1040 (or BStD1040)
1	Z-diode	BZX 83/C15
1	Diode	1N4005
1	Electrolytic capacitor	2.2 μ F/25 V
1	Resistor	3.9 k Ω /0.5 W
1	Resistor	10 k Ω /0.5 W
1	Resistor	560 k Ω /0.5 W

Components for circuit 7.6.6

1	to n Opto couplers	SFH 600/II
1	to n Thyristors trigger class S2	BStC1040 (or BStD1040)
1	Z-diode	BZX 97/C12
1	Diode	1N4001
1	MKT-capacitor	0.68 μ F/100 V
1	Electrolytic capacitor	220 μ F/16 V

Components for circuit 7.6.7

1	Opto coupler	SFH 600/II
1	Triac, trigger class K	TX C 1040 (or TX D 1040)
1	Transistor	BC 238 B
1	Z-diode	BZX 83/C15
1	Diode	BAY 61
1	MKT-capacitor	0.15 μ F/630 V
1	Electrolytic capacitor	47 μ F/25 V
1	Resistor	220 Ω /0.5 W
1	Resistor	1 k Ω /0.5 W
1	Resistor	6.8 k Ω /0.5 W

Components for circuit 7.6.8

For permanent pulse control:

		Ordering code
1	Opto coupler SFH 600/III	Q68000-A5055
1	Triac, trigger current ≤ 10 mA TX C 1040 (or TX D 1040)	C67048-A1505-A2
1	Z-diode BZY 97/C12	Q68000-A955-F82
1	Diode 1N4001	C66047-Z1306-A21
1	MKT-capacitor 0.6 μ F/250 V~	B32655-J6684-K
1	Electrolytic capacitor 220 μ F/16 V	B41283-B4227-T
1	Resistor 120 Ω /0.5 W	B51261-Z4121-J1
1	Resistor 390 Ω /0.5 W	B51261-Z4391-J1

For long pulse control

1	Opto coupler SFH 600/III	Q68000-A5055
1	Triac, trigger current=10 mA TX C 1040 (or TX D 1040)	C67048-A1505-A2
1	Z-diode BZY 97/C12	C68000-A955-F82
1	Diode 1N4001	C66047-Z1306-A21
1	MKT-capacitor 0.1 μ F/250 V~	B32655-J6104-K
1	Electrolytic capacitor 22 μ F/25 V	B41313-A5226-T
1	Resistor 120 Ω /0.5 W	B51261-Z4121-J1
1	Resistor 390 Ω /0.5 W	B51261-Z4391-J1



7.7 Contactless Electronic Control for Rotational Speed of Fans

Electronic devices and systems, which are equipped with fans for cooling, very often operate with bimetal sensors for temperature monitoring. Thus an inadmissibly high air temperature or a too high temperature generation inside of the equipment is reliably recognized as long as the fan runs at rated rotational speed. If the fan, however, fails because of an interruption of the motor circuit or due to a bearing damage or if the rotational speed of the fan decreases due to a beginning bearing defect, the air convection is reduced so strongly that the bimetal sensors do not or too late react. This results in functional troubles by, e.g., thermally overloaded semiconductors. A safe protection is realized by additional monitoring of the fan rotational speed.

The controller for the rotational speed consists of a magnetic barrier as speed sensor (permanent magnet and Hall-IC) and an electronic processing circuit.

The development of this circuit is based on the assumption to sense the rotational speed of the fan without any additional mechanical elaborateness.

A small permanent magnet (VACOMAX® of Vacuum Schmelze GmbH, Hanau) is glued on the fan rotor. The processing circuit including the Hall-IC SAS 251 and being mounted on a pc board is centred over the rotating fan axis by a fixing bow. At every rotation the Hall-IC supplies a pulse to the processing circuit.

Fig. 7.7.1 shows the circuit of the rotational speed controller. TCA 955 comprises all necessary components for realizing the switching with the exception of those for output stage, Hall-IC and dead-time circuit.

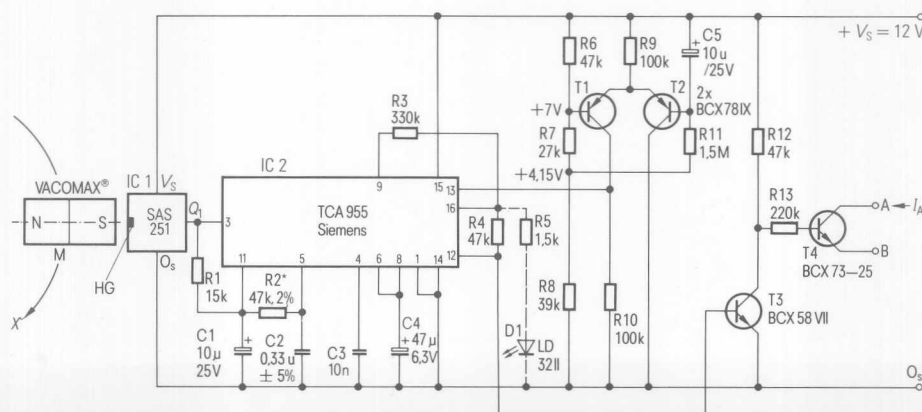


Fig. 7.7.1

The pulses generated by the Hall-IC SAS 251 are converted to a dc voltage being proportional to the rotational speed. The next step is the comparison of desired and actual value. The Schmitt-trigger supplies a signal with H-level when the rotational speed of the fan is lower than $n=2000$ rpm. In this case the LED-display for failure indication is turned on, too. The dead-time circuit is provided for keeping the output stage conductive by means of an interlocking circuit during starting of the fan (approx. 7 s). Thus a failure signal is not generated.

The desired value of the rotational speed is determined by the time circuit consisting of R_2 , C_2 and by the thresholds of the IC.

A dc voltage being proportional to the rotational speed is available at filter capacitor C_4 . It is imposed by a triangular voltage with a peak to peak value of approx. 60 mV. To get unambiguous switching states, a hysteresis is realized by feedback resistor R_3 .

For easy servicing every controller board is equipped with an LED, indicating a fan failure. The LED emits light also during the short starting of the fan.

The dead-time circuit comprises the differential amplifier with T_1 , T_2 and the time circuit with R_{11} and C_5 . Transistor T_1 is conductive when the supply voltage is applied. The comparator (battery voltage indicator) of the TCA 955, input at pin 13 and output at pin 12 are conductive and therefore the output stage is blocked. After a certain delay time the output stage is released.

Up to 24 output stages as well as additional bimetal sensors can be connected in series. They are only controlled by a comparator of the central monitoring device as shown in **fig. 7.7.2**. Under normal conditions all outputs are conductive, i.e., an alarm is released when a line is interrupted.

At series connection collector and base current of the last transistor have to be supplied by the output transistor.

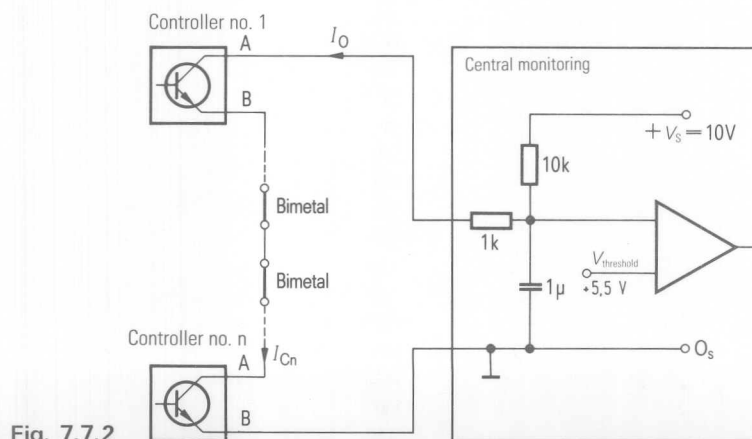
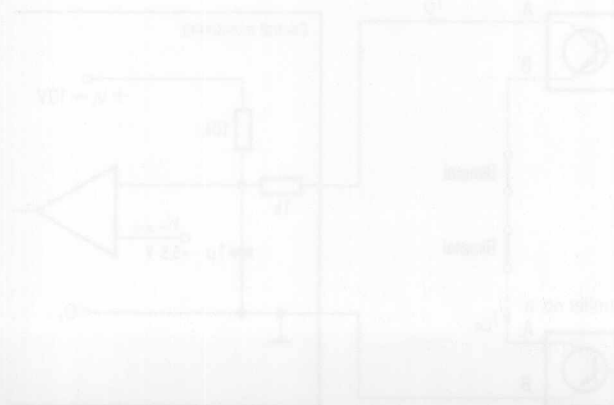


Fig. 7.7.2

The residual voltage of transistor BCX 73-25 is <150 mV. Therefore the 5.5-V-threshold of the main comparator is not exceeded with 24 output stages.

Components for circuit 7.7.1

			Ordering code
1	Magnetically operated contactless switch with static outputs	SAS 251	Q67000-S47
1	Window discriminator	TCA 955	Q67000-A983
1	Silicon-NPN-Transistor	BCX 58 VII	Q62702-C618
1	Silicon-NPN-Transistor	BCX 73-25	Q62702-C634-S2
2	Silicon-PNP-Transistors	BCX 78 IX	Q62702-C628
1	Diode TSN-LED, red,	LD 32 II, 3 mm	Q62703-Q175
1	Ceramic multi-layer capacitor	10 nF	B37981-J5103-K
1	MKT-(MKH)-layer capacitor	0.33 μ F, 100 V	B32560-D1334-J
2	Tantalum electrolytic capacitors	10 μ F, 25 V	B45181-B3106-M
1	Tantalum electrolytic capacitor	47 μ F, 6.3 V	B45181-A0476-M
13	Carbon layer resistors	0.33 W $\pm$ 5%	B51261-Z4...-J1
1	Permanent magnet VACOMAX®, 6 mm $\times$ 6 mm $\times$ 2.5 mm, Magnetization in direction of the 2.5 mm-edge		Fa. Vacuumschmelze GmbH, Hanau



7.8 Electronic Control for Universal Motors with Excess Temperature Control and Starting Current Limitation

Greater universal motors with an active power of 500 to 1000 W often require such a high starting current that the fuse blows.

Fig. 7.8 shows a circuit which slowly increases the starting current by a phase angle controller from zero to a desired value. For the phase angle control the IC TCA 780 is utilized. The synchronizing signal is derived from the mains voltage and applied via a 1 M Ω -resistor to pin 5. An incorporated detector senses every zero-axis crossing. Its output signal is supplied to a synchronization register.

The latter controls a ramp generator which charges capacitor C_3 by a constant current being determined by resistors R_1 and R_2 . When the ramp voltage at pin 10 exceeds the control voltage at pin 11 (switching point φ) a signal is supplied to the logic. The switching point φ can be shifted within a phase angle of 0° and 180° in dependence on the control voltage at pin 11.

At outputs 14 and 15 a positive pulse with a duration of approx. 370 μ s is available at every half wave. The trigger pulse length is determined by the capacitance of C_4 . The outputs can be blocked by a signal applied to inhibit input 6.

After the turn-on the smoothing capacitor C_1 is relatively fast charged and a supply voltage of 12 V is applied to the IC. Capacitor C_2 is not charged as fast as C_1 because its minus-pole is connected to ground via a 15 k Ω -resistor being incorporated to the IC.

Therefore the control voltage level is kept higher than the one of the saw-tooth signal at pin 10 as long as the supply voltage is totally available.

Thereafter the charging to the desired control voltage level starts (phase control angle α).

The transistor is turned off, when the control voltage is decreased by the 22 k Ω -potentiometer. In this case α increases and the variation follows delayed by the charging time constant of capacitor C_2 .

When the control voltage is increased the transistor is turned on and the capacitor C_2 is relatively fast discharged. The transistor current is limited by the collector resistor. In this case α is decreased.

The voltage divider connected to inhibit input at pin 6 is responsible for turning off the triac, i.e. the motor, when the motor temperature exceeds approx. 100 °C. A half-wave operation is realized at a slow change over.

When dimensioning the circuit the following has to be considered:

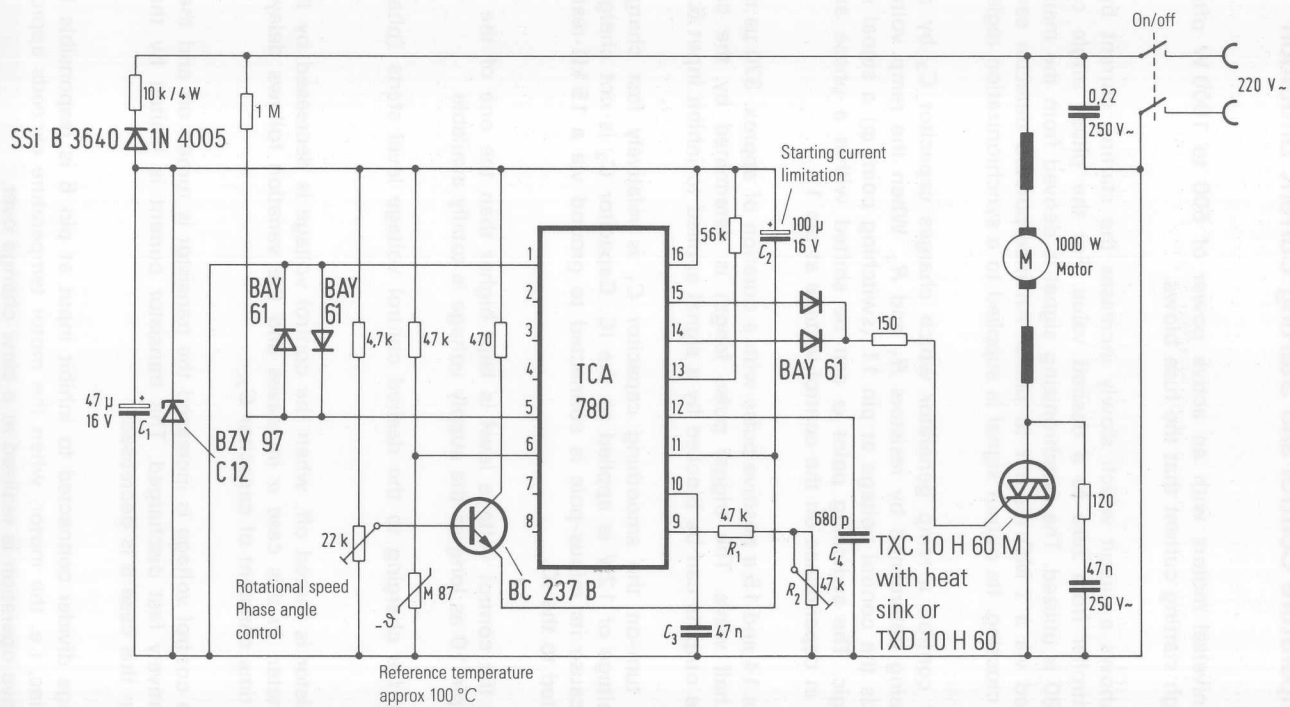


Fig. 7.8

If the capacitance of C_1 is higher than indicated in fig. 7.8 the following effect is generated, when the circuit is turned on and off with a relatively high frequency. The triac is fired during the positive half wave much below the adjusted value, as the triggering sensitivity is higher for positive pulses. Then smaller phase control angles α are generated and when the supply voltage for the IC is increased to its final level the originally desired value for α is reached again.

The cause for this effect is as follows. The saw-tooth signal of the ramp generator cannot be generated as fast as necessary. It is limited by the supply voltage being still too low. The result is in that a wrong information is supplied to the pulse logic circuit.

Components for circuit 7.8

		Ordering code
1 Phase control IC	TCA 780	Q67000-A1087
1 Triac with heat sink or	TXC 10H60M	C66048-A1505-A9
1 Triac with heat sink	TXD 10H60	C66048-A1504-A8
1 Z-diode	BZY 97C12	Q68000-A955-F82
1 Diode	1 N 4005	C66047-Z1306-A25
1 Transistor	BC 237 B	Q62702-C277
4 Diodes	BAY 61	Q62702-A389
1 NTC resistor	M 87/20%/200 k Ω	Q63087-M204-M
1 Polypropylene capacitor	680 pF/160 V	B33063-B1681-H
1 MKT-layer capacitor	47 nF/100 V	B32510-D3473-K
1 MKT-layer capacitor	47 nF/250 V~	B32655-J6473-K
1 MKT-layer capacitor	0.22 μ F/250 V	B32655-J6224-K
1 Electrolytic capacitor	47 μ F/16 V	B41283-B5476-T
1 Electrolytic capacitor	100 μ F/16 V	B41283-B4107-T
1 Resistor	120 Ω /0.5 W	B51261-Z4121-J1
1 Resistor	150 Ω /0.5 W	B51261-Z4151-J1
1 Resistor	470 Ω /0.5 W	B51261-Z4471-J1
2 Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	10 k Ω /4 W	B56675-A2103-J
1 Resistor	47 k Ω /0.5 W	B51261-Z4473-J1
1 Resistor	56 k Ω /0.5 W	B51261-Z4563-J1
1 Resistor	1 M Ω /0.5 W	B51261-Z4105-J1

7.9 Rectifier Operation with Semi-Controlled Single-Phase Bridge Circuit and Optoelectronic Couplers

Semi-controlled single-phase bridge circuits are equipped with half of thyristors and half of diodes. The advantage in comparison to fully controlled single-phase bridge circuits is in that the number of required thyristors is reduced by 50%. Besides that the dc current ripple is much lower and the mains is less loaded by the reactive control power.

The semi-controlled bridge circuit can be considered as series connection of two Mp-circuits one being controlled, the other not. This causes a sequential control within a current rectifier circuit. There are balanced as well as unbalanced semi-controlled single-phase bridge circuits. At the former only one bridge side is controlled, at the latter, however, only one branch of each side is controlled. The advantage of the unbalanced semi-controlled bridge circuit is in that the current at an inductive load flows via the two other uncontrolled rectifiers, even after cut-off by the thyristors until the energy stored in the coil is dissipated. In this case a protection diode connected in parallel to the inductor is not necessary.

At the interface of the controller and the main current circuit there are problems with the different potentials of both circuits. Therefore control circuits for thyristors have to consider these potential differences. This can be achieved by using optoelectronic couplers which galvanically separate controller and power switch circuit.

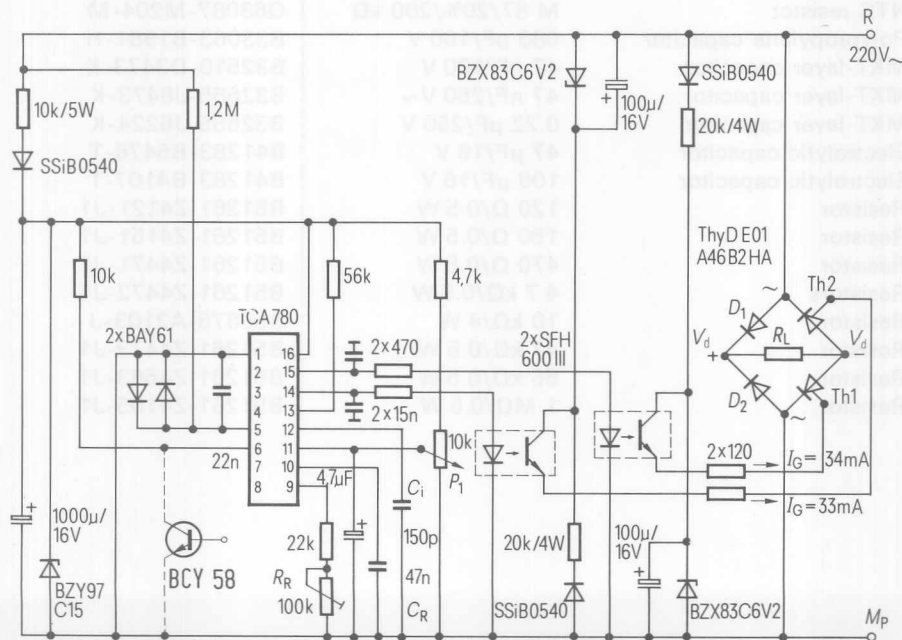


Fig. 7.9

Fig. 7.9 shows a circuit using the phase control IC TCA 780. The power dissipation of the dc load can be continuously controlled.

100 sinusoidal half waves, being phase-angle controlled, are available at the dc current output. The control circuit is similar to the one described in section 7.8. The power stage of the bridge comprises the new-designed compact modules Thy D E01.

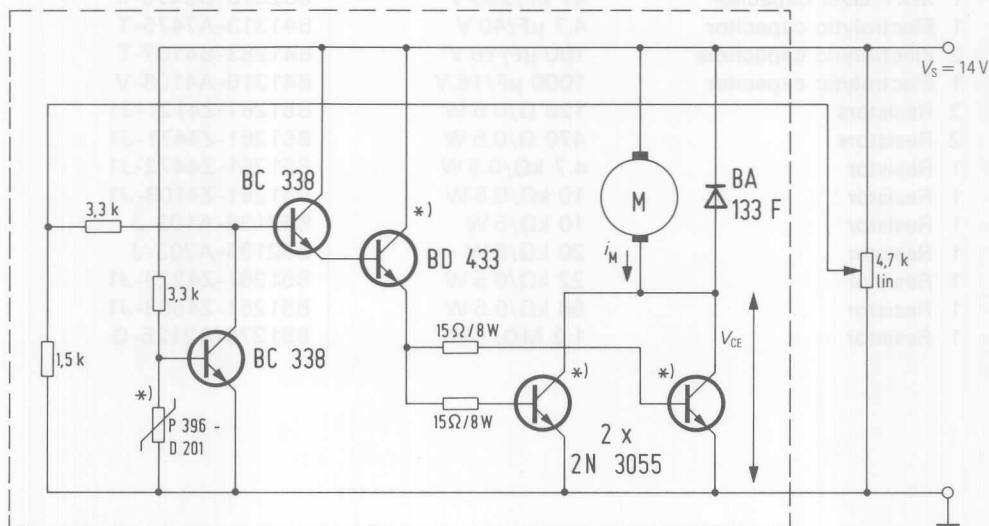
Dc loads with a power dissipation of up to 3 kW can be operated if the thermal resistance of the heat sink is 0.2 K/W.

Components for circuit 7.9

			Ordering code
1 Phase control IC	TCA 780		Q67000-A1087
1 Compact module	Thy D E01 A46 B2HK		Q67067-A1801-A105
1 Transistor	BCY 58		Q60203-Y58
2 Opto couplers	SFH 600 III		Q68000-A5055
2 Z-diodes	BZX 83/C6V2		Q62702-Z1072-F82
1 Z-diode	BZY 97/C15		Q68000-A957-F82
2 Rectifier diodes	SSi B0540		C66047-A1005-A4
2 Diodes	BAY 61		Q62702-A389
1 Ceramic capacitor	150 pF/63 V		B38062-J6151-G6
2 MKT-layer capacitors	15 nF/400 V		B32510-D6153-K
1 MKT-layer capacitor	22 nF/250 V		B32510-D3223-K
1 MKT-layer capacitor	47 nF/250 V		B32510-D3473-K
1 Electrolytic capacitor	4.7 μ F/40 V		B41313-A7475-T
2 Electrolytic capacitors	100 μ F/16 V		B41283-B4107-T
1 Electrolytic capacitor	1000 μ F/16 V		B41316-A4108-V
2 Resistors	120 Ω /0.5 W		B51261-Z4121-J1
2 Resistors	470 Ω /0.5 W		B51261-Z4471-J1
1 Resistor	4.7 k Ω /0.5 W		B51261-Z4472-J1
1 Resistor	10 k Ω /0.5 W		B51261-Z4103-J1
1 Resistor	10 k Ω /5 W		B52136-A103-J
1 Resistor	20 k Ω /5 W		B52136-A203-J
1 Resistor	22 k Ω /0.5 W		B51261-Z4223-J1
1 Resistor	56 k Ω /0.5 W		B51261-Z4563-J1
1 Resistor	1.2 M Ω /1 W		B51276-A2125-G

7.10 Electronic Control for Rotational Speed of Blower with Full Load Current of 20 A

The circuit shown in **fig. 7.10** is suited for a full load current of 20 A. It is dimensioned in that a small residual voltage drops across the control component at current maximum. Therefore two transistors, type 2 N 3055, are connected in parallel. They are controlled via two separate base resistors. The required base current is supplied by two transistors BC 338 and BD 433, operating as common-emitter circuits and connected in series. The motor current and thus the rotational speed depend on the tap position of the 4.7-k Ω -potentiometer. If the power transistors are commonly mounted on a cooling block and if they are directly exposed to the blower air blast, the excess temperature maximum at the cooling block is limited by a value of less than 30 K. When the rotational motor speed is slowed down by external force in that the cooling air blast is interrupted, the thermal overload protection reacts. When the temperature of the cooling block exceeds 120 $^{\circ}$ C, the resistance of the PTC resistor, being in thermal contact with the cooling block, increases drastically. The lower transistor BC 338 becomes conductive and the upper one is shunted, that means it is blocked.



*) commonly mounted on a cooling block being exposed to the air blast of the blower

Fig. 7.10

Components for circuit 7.10

		Ordering code
2 Transistors	2N3055	Q62702-U58-F14
1 Transistor	BD 433	Q62702-D201
2 Transistors	BC 338	Q62702-C314
1 Diode	BA 133 F	Q62702-A505-F4
1 PTC resistor	P 396-D210	Q63100-P396-D201
2 Resistors	15 Ω /8 W	B52137-A150-J
1 Resistor	1.5 k Ω /0.5 W	B51261-Z4152-J1
2 Resistors	3.3 k Ω /0.5 W	B51261-Z4332-J1

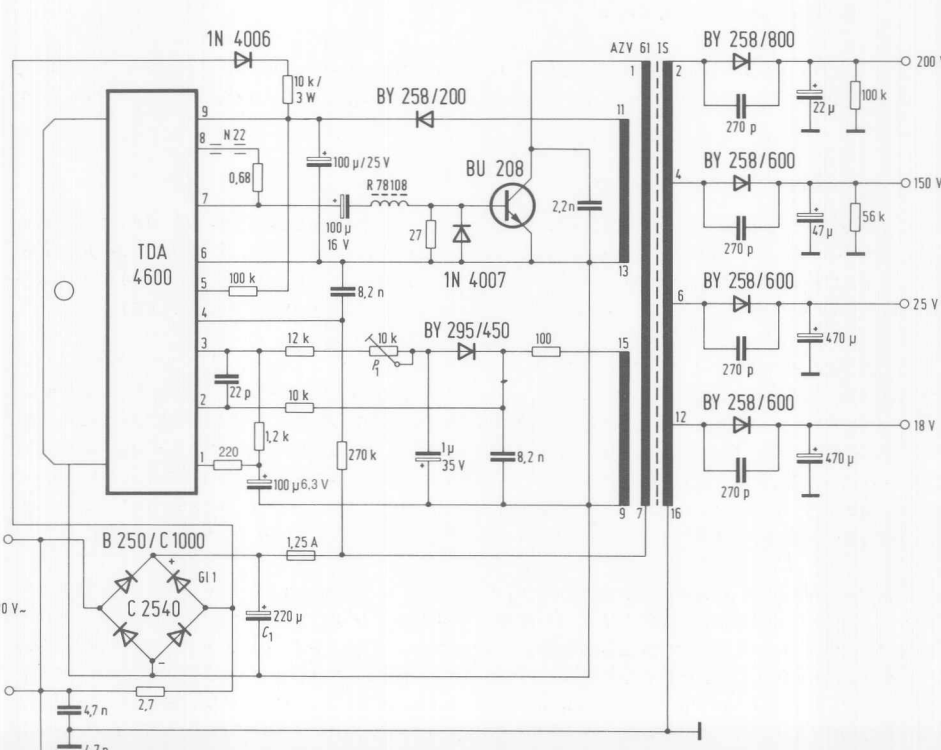
TDA 4600

d operation.

A 4600 offers a wide control range and a

ns voltage is rectified by bridge rectifier G11

voltage is periodically applied to windings



During the inverse period of the BU 208 voltage peaks are generated at secondary windings 2 to 16. They are rectified by four diodes, type BY 258, and thus the supply voltage of 150 V is generated. It is adjustable by potentiometer P_1 .

Load variations at the 18 V and 25 V-outputs have only a small influence to the stability of the 150 V-voltage because of special arrangement of the feedback windings 9 to 15 and due to a special dimensioning.

Starting behaviour

There are three operating modes during the start (turn on).

- 1st: Generating an internal reference voltage for supplying the voltage regulator and for charging the coupling 100 μ F-capacitor.
- 2nd: Enabling the internal supply voltage-reference voltage $V_1 = 4$ V. This voltage is immediately turned on when the voltage $V_9 \approx 12$ V is switched on. It is responsible for all stages of the IC with the exception of the control logic. This supply voltage is over-load protected and thermally regulated.
- 3rd: Enabling of the control logic. Besides the reference voltage the supply voltage for the control logic is switched on by an additional regulating circuit, i.e. the IC is ready to operate.

This starting procedure is necessary to guarantee the charging of the coupling 100 μ F-capacitor. In this case an accurate switching of transistor BU 208 is only obtained.

Standard operation/controlling

The zero-axis crossings of the signal applied to the input (pin 2) are counted. Then this information is processed and supplied to the control logic circuit. The rectified amplitude variations of the signal from the feedback winding are applied to pin 3 which is the input for the overload, control and stand-by control.

The control amplifier operates with an input voltage of approx. 2 V at a transverse current of ≈ 1 mA. The overload control circuit limits the dynamic range in dependence on two internal reference voltages by means of the balancing network for the collector current. This circuit imitates the collector current by an internal reference voltage and by an external RC-network connected to pin 4. In the described example the network capacitance is 8.2 nF, but when it is increased the collector current maximum of the switching transistor is also increased (turning point).

Thus the required control range being between a dc level of 2 V and a sawtooth signal with a maximum of 4 V (reference voltage) is set. The oscillating frequency is increased to a value of about 50 kHz when the secondary load is decreased to a minimum of approx. 20 Watt. The duty cycle of approx. 0.3 remains nearly constant. But the duty cycle changes to a value of approx. 0.09 when the load decreases to a value of approx. 1 Watt. In this case the frequency also changes to approx. 70 kHz. Besides that the collector peak current is reduced to less than 1 A.

The trigger circuit compares the output signals of the control amplifier of the load control and of the balancing network for the collector current. Then these signals are supplied to the control logic. Pin 5 offers an additional trigger and blocking possibility. When the voltage at this input is $\leq 2.2\text{ V}$ the output at pin 8 is turned off.

The flip-flop circuits which control base-current amplifier and limiter are set in dependence on the starting circuit, the zero-crossing identification, the collector-current balancing network and the trigger enabling. The base-current amplifier processes the saw-tooth voltage in that V_4 is available at the output (pin 8). Between pins 8 and 7 a current-feedback resistor ($R \approx 0.68\ \Omega$) is connected. The resistance determines the amplitude maximum of the base control current for the switching transistor.

Protected operation

The base-current limiter, being influenced by the control logic, clamps the output voltage at pin 7 to a level of 1.6 V. Thus the switching transistor is blocked. This protective measure is released when either the supply voltage at pin 9 has a value of $\leq 7.0\text{ V}$ or the voltages at pin 5 are $\leq 2.2\text{ V}$. When a short-circuit of the secondary windings occurs the IC controls itself by a continuous scanning. At open-loop operation of the secondary winding the duty cycle of the oscillating signal is small. In both cases the total power dissipation N of the switch mode power supply is between 6 and 10 W. The output is turned off when the supply voltage V_9 is less than 7.0 V. When V_9 is further decreased to a value of 6 V the reference voltage of 4 V is turned off.

Before replacing the TDA 4600 it has to be ensured that capacitor C_1 is discharged.

Components for circuit 8.1

		Ordering code
1 Control-IC for SMPS	TDA 4600	Q67000-A1451
1 Transistor	BU 208	Q68000-A494
1 Bridge rectifier	C 2540 B 250	C66067-A1735-A5
	C 1500/1000	
1 Diode	BY 258/200	C66047-A1071-A7
3 Diodes	BY 258/600	C66047-A1071-A4
1 Diode	BY 258/800	C66047-A1071-A8
1 Diode	BY 259/450	C66047-A1063-A6
1 Diode	1 N 4006	C66047-Z1306-A26
1 Diode	1 N 4007	C66047-Z1306-A27
1 Ceramic capacitor	22 pF	B38116-J5220-J1
4 Ceramic capacitors	270 pF	B37370-A2271-K3
1 MKP-capacitor	2.2 nF/1500 V	B32650-J1222-K
2 MKT-capacitors	8.2 nF/250 V	B32560-D3822-K
7.5 mm-pin distance		
1 MKP-capacitor	0.68 μ F/400 V	B32650-J4684-K
1 Electrolytic capacitor	1 μ F/40 V	B41315-A-7105-V
1 Electrolytic capacitor	22 μ F/350 V	B43052-V-4226-T
1 Electrolytic capacitor	47 μ F/250 V	B43052-V-2476-T1
1 Electrolytic capacitor	100 μ F/6.3 V	B41316-A-2107-V
1 Electrolytic capacitor	100 μ F/16 V	B41316-A-4107-V
1 Electrolytic capacitor	100 μ F/25 V	B41283-B-5107-T
1 Electrolytic capacitor	220 μ F/385 V	B43306-B-4227-T
1 Electrolytic capacitor	470 μ F/25 V	B41012-A-5477-T
1 Electrolytic capacitor	470 μ F/40 V	B41012-A-7477-T
1 Ferrite bead		B62110-A-5028-X25
1 Blocking oscillator transformer	AZ 56120	—
1 Potentiometer, horizontally mounted	10 k Ω	B58054-Z103-M300
1 Choke	4.7 μ H	B78108-S-1472-K
1 Resistor	0.68 Ω /0.5 W	—
1 Resistor	2.7 Ω /4 W	—
1 Resistor	27 Ω /0.4 W	B54311-Z5270-G1
1 Resistor	100 Ω /3 W	—
1 Resistor	220 Ω /0.4 W	B54311-Z5221-G1
1 Resistor	1.2 k Ω /0.5 W	B51261-Z4122-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	10 k Ω /3 W	B52135-A2103-J
1 Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
1 Resistor	56 k Ω /0.5 W	B51261-Z4563-J1
2 Resistors	100 k Ω /0.5 W	B51261-Z4104-J1
1 Resistor	270 k Ω /0.5 W	B51261-Z4274-J1

8.2 Half Bridge Switch Mode Power Supply Using TDA 4700

Half bridge switch mode power supplies (SMPS) meet an increasing popularity in their application as switching transistors with relatively low voltage characteristics are required and as the efficiency of the power transformer is high. In the circuit shown in **fig. 8.2** the transformer Tr1 is directly connected to capacitor C_{sym} to compensate a premagnetization of the transformer core generated due to unsymmetries of the circuit. If conventional push-pull or full-bridge circuits are used the premagnetization effect can be prevented by a symmetrical circuit connected to pins 6 and 24 of the IC.

The switching power transistors are driven by two transformers. They are operated by transistors T_1 and T_2 , being directly connected to the IC TDA 4700.

The circuit is dimensioned for a resonant frequency of 40 kHz and the IC can be operated in a free-running or synchronous mode as required. The sync output serves as a master for several SMPSs connected in parallel.

The collector currents of the power transistors are transferred by the current converter Tr4, that means there is a galvanic isolation. When the admissible collector current is exceeded the comparator, being part of the IC, immediately cuts off the power output stages for the duration of a half oscillation cycle.

The output voltage being set to a reference of 2.5 V is controlled by the voltage divider consisting of resistors R_8 , R_9 and R_{10} . When the output voltage is exceeded, the switching power supply is turned off. The influence of components tolerances is compensated by potentiometer R_9 .

The output voltage is set by resistors R_6 and R_7 . When it is exceeded for more than 10% the SMPS is turned off by another comparator of the IC as long as the auxiliary voltage is switched off for a short time or as input 21 is briefly connected to ground. Without connection to pin 21 and 20 the SMPS automatically turns on, when the excess voltage has been reduced to a normal value.

A precontrol for mains hum suppression can be realized by applying the interference voltage to pin 21 of the ramp generator. This control requires the transfer of an analog signal, e.g. with compensated opto couplers. But in this application example it is not used.

Transformer Tr5 and rectifier G12 generate an auxiliary voltage which is controlled by the comparator being responsible for input undervoltages. Besides that the IC can be turned on or off by a remote-controlled signal applied to this input.

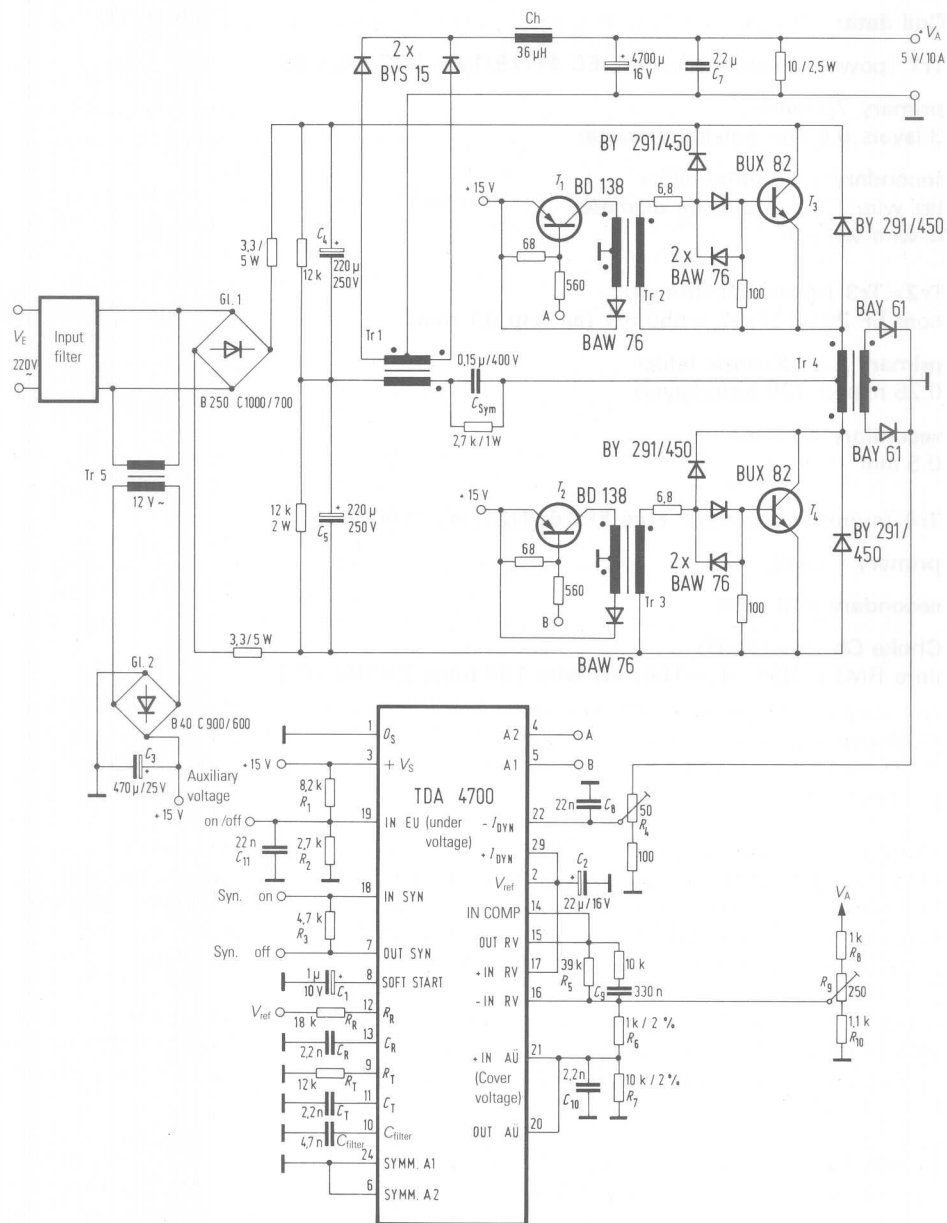


Fig. 8.2

Coil data:

Tr1 (power transformer): core EC 41/19/12 – N27; $A_L=530$

primary 75 turns

3 layers 0.6 mm outside diameter

secondary 2×5 turns bifilar

litz wire 1.2 mm outside diameter

4-wire wound

Tr2=Tr3 (driver transformer):

core EF 25; N27; $A_L=550$ nH (air gap 0.1 mm)

primary 2×100 turns bifilar

0.25 mm $\varnothing$ (28 turns/layer)

secondary 23 turns

0.5 mm

Tr4 (current converter): core EF 16; N27; $A_L=1000$ nH

primary 6 turns

secondary 240 turns

Choke Ch ($L=36$ μ H)

core RM12, N41; $A_L=160$; litz wire 156 turns $2 \times 100 \times 0.1$

Components for circuit 8.2

		Ordering code
1 Control IC for SMPS	TDA 4700 A	Q67000-Y594
2 Transistors	BD 138	Q62702-D109
2 Transistors	BUX 82	Q68000-A4676
1 Bridge rectifier	B250 C 1000/700	C66067-A1706-A4
1 Bridge rectifier	B40 C 900/600	C66067-A1751-A3
2 Diodes	BAY 61	Q62702-A389
6 Diodes	BAW 76	Q62702-A397
4 Diodes	BY 291/450	C66047-A1044-A6
2 Diodes	BYS 15	C67047-Z1318-A1
2 MKT-layer capacitors	2.2 nF/400 V	B32560-D6222-J
1 MKT-layer capacitor	4.7 nF/400 V	B32560-D6472-J
2 MKT-layer capacitors	22 nF/250 V	B32560-D3223-J
1 MKT-layer capacitor	330 nF/100 V	B32560-D1334-J
1 MKT-layer capacitor	0.15 μ F/400 V	B32562-D6154-J
1 Al-electrolytic capacitor	1 μ F/100 V	B41313-A9105-T
1 MKT-layer capacitor	2.2 μ F/250 V	B32563-D3225-J
1 Ta-electrolytic capacitor	33 μ F/10 V	B45181-B1336-M
2 Al-electrolytic capacitors	220 μ F/250 V	B43306-B2227-T
1 Al-electrolytic capacitor	470 μ F/25 V	B41010-B5477-T
1 Al-electrolytic capacitor	4700 μ F/16 V	B41010-C4478-T
2 Resistors	3.3 Ω /5 W	B52136-A030-J300
2 Resistors	6.8 Ω /0.4 W	B54311-Z5060-G801
1 Resistor	10 Ω /2.5 W	B52135-A4100-J
2 Resistors	68 Ω /0.5 W	B51261-Z4680-J1
2 Resistors	100 Ω /0.5 W	B51261-Z4101-J1
2 Resistors	560 Ω /0.5 W	B51261-Z4561-J1
2 Resistors	1 k Ω /0.5 W/5%	B51261-Z4102-J1
1 Resistor	1 k Ω /0.5 W/2%	B51261-Z4102-G1
1 Resistor	2.7 k Ω /0.5 W	B51261-Z4272-J1
1 Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
1 Resistor	8.2 k Ω /0.5 W	B51261-Z4822-J1
1 Resistor	10 k Ω /0.5 W/5%	B51261-Z4103-J1
1 Resistor	10 k Ω /0.5 W/2%	B51261-Z4103-G1
1 Resistor	12 k Ω /0.5 W	B51261-Z4123-J1
2 Resistors	12 k Ω /2 W	B52135-A123-J
1 Resistor	33 k Ω /0.5 W	B51261-Z4333-J1
1 Resistor	39 k Ω /0.5 W	B51261-Z4393-J1
1 Transformer core	EC 41/10/12	B66339-G0250-X127
1 Transformer core	EF 25	B66317-G0100-X127
1 Transformer core	EF 16	B66307-G0000-X127
1 Choke core	RM 12	B65815-J0160-A041

8.3 Parallel-Connected Voltage Regulators

Usually voltage regulators cannot be connected in parallel as too great current differences exist because of the reference voltage tolerances of the IC. But with an accurate selection a parallel operation is possible.

A simple solution is demonstrated by the circuit of **fig. 8.3**. In this case a balancing is obtained by the symmetry potentiometer connected to the reference input of the ICs. A current selection is absolutely not necessary, but the output voltage becomes a little bit weaker.

A 0.1 μF -capacitor is connected to each IC to suppress undesired oscillations. Without these capacitors an abrupt hysteresis characteristic is obtained at load variations.

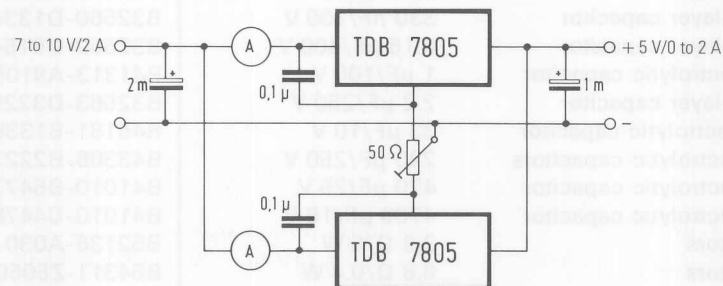


Fig. 8.3

Components for circuit 8.3

		Ordering code
2 Voltage regulators, e.g.	TDB 7805 T	Q67000-A1048
2 MKT-layer capacitors	0.1 μF /100 V	B32560-D1104-J
1 Electrolytic capacitor	1 mF/6 V	B41283-A2108-T
1 Electrolytic capacitor	2 mF/16 V	B41010-E4228-T

8.4 Power Supply for Microcomputer Systems

Fig. 8.4.1 shows a circuit for a power supply, being rated for 5 V/2 A, +12 V/0.5 A, -12 V/0.5 A and 24 V/0.25 A. It operates at mains voltages of 220 V and 110 V (50 Hz). A 100 nF-capacitor is connected between the two input lines to eliminate interferences being dropped in from the mains. The voltage supply circuits for 5 V and 12 V operate with integrated constant-voltage regulators. Every input is by-passed by a 0.33 μ F-capacitor to avoid undesired oscillations. In some cases it is also necessary to protect the outputs by capacitors. The circuit for the regulated output voltage of 5 V offers a supply current of 2 A. It operates with two parallel-connected voltage regulators. A 50 Ω -potentiometer is connected between the two lines for the minus reference voltage to avoid unsymmetrical currents. The four secondary voltages are rectified by Silicon bridge-rectifiers. The data for transformers and coils (winding schematic, see fig. 8.4.2) is as follows:

Transformer data Tr1:

C-core:	SM 65
Magnetic flux density:	1.6 T=16 kGs
Specific turns/volt:	5.45 t/V

Secondary windings for	{	5 V/2 A	(n1)/5 to 6=54 turns/2 $\times$ 0.60 $\varnothing$ ECu
	{	12 V/0.5 A	(n2)/3 to 4=86 turns/0.45 mm $\varnothing$ ECu
	{	12 V/0.5 A	(n3)/7 to 8=86 turns/0.45 mm $\varnothing$ ECu
	{	24 V/0.5 A	(n4)/1 to 2=110 turns/0.55 mm $\varnothing$ ECu
Primary windings for	{	110 V	(n5)/9 to 11=600 turns/0.32 mm $\varnothing$ ECu
	{	110 V	(n6)/10 to 12=600 turns/0.32 mm $\varnothing$ ECu

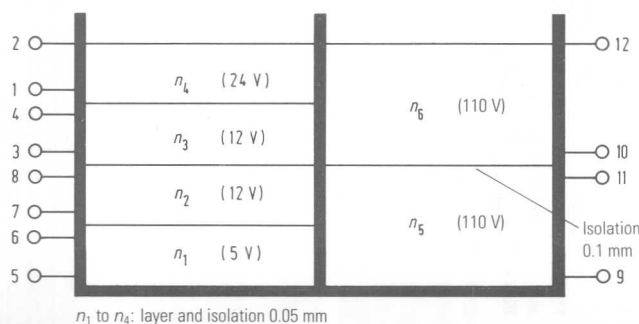
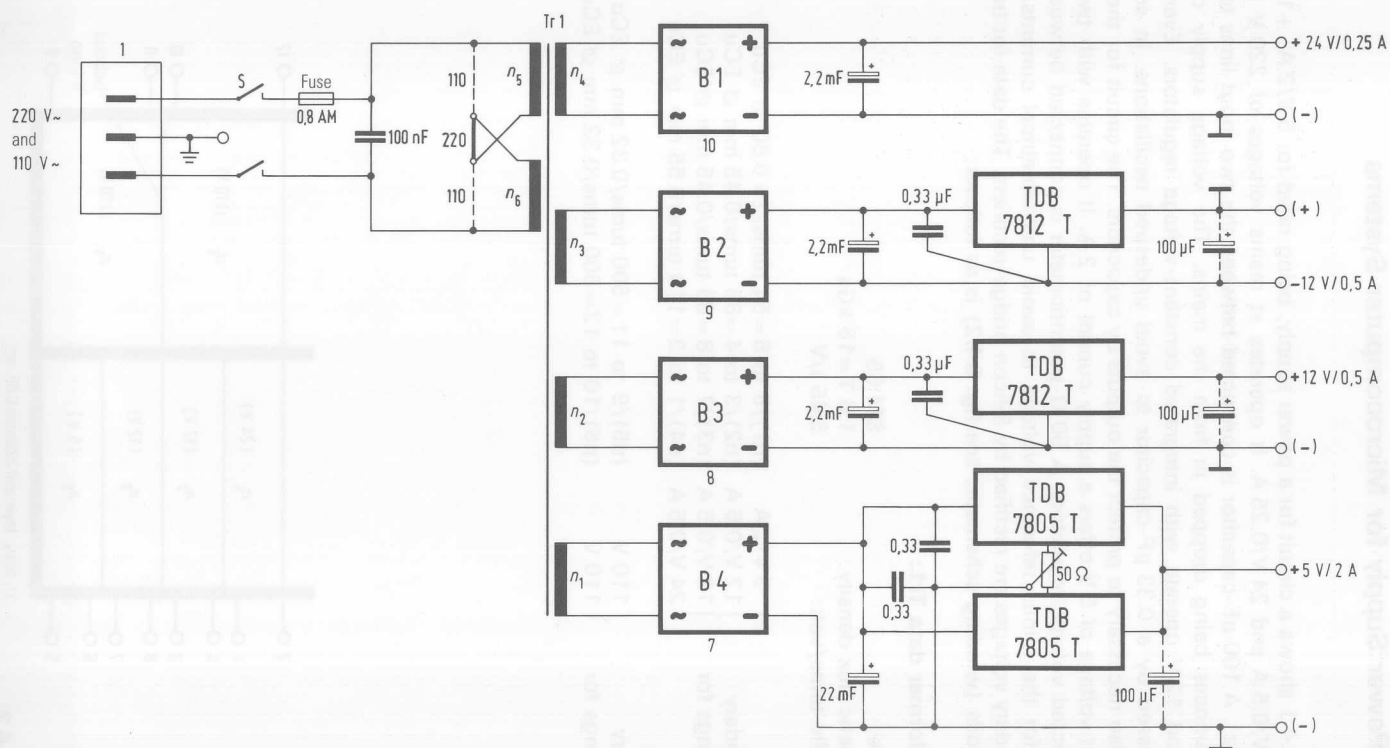


Fig. 8.4.2

Fig. 8.4.1



Components for circuit 8.4

		Ordering code
2 Voltage regulators	TDB 7805 T	Q67000-A1048
2 Voltage regulators	TDB 7812 T	Q67000-A1057
1 Transformer in accordance to construction requirements	Tr1	—
1 Bridge rectifier	B 40 C 5000/3300	E2106-B40-C5000/3300
3 Bridge rectifiers	B 40 C 1500/1000	B1906-B40-C1500/1000
1 Capacitor	100 nF/250 V	B81111-B-B26
4 MKT-layer capacitors	0.33 μ F/100 V	B32560-D1334-J
3 Electrolytic capacitors	100 μ F/16 V	B41283-B4107-T
2 Electrolytic capacitors	2.2 mF/25 V	B41293-J5228-T
1 Electrolytic capacitor	2.2 mF/40 V	B41293-B7228-T
1 Electrolytic capacitor	22 mF/16 V (vertical)	B41306-K4229-T
1 Potentiometer	50 Ω /0.3 W	
1 Fuse	0.8 A M	

8.5 20 kHz-Thyristor Switching Regulator with Output Voltage Controllable between 0 and 30 V

The circuit described in the following operates with a fast switching thyristor as a controlled rectifier. It is directly connected to the secondary winding of a 20 kHz-converter. In this case the commonly used rectifier diodes are not necessary. A constantly adjustable output voltage from 0 V up is obtained with a high stability by controlling the phase angle of the secondary voltage. The efficiency is 60% to 75% in dependence on the load.

The input power required for this switching regulator is applied by an external generator with a fixed frequency of 20 kHz. It supplies sine-wave, trapezoidal or square-wave voltages. Its dimensioning is not subject of this description and it is assumed that the secondary winding of transformer Tr1 delivers the desired voltages and currents. The generator voltage itself may be unregulated. A short-circuit-proof operation is realized by the following switching regulator.

The circuit shown in **fig. 8.5** is dimensioned for voltages between 0 and 30 V at an output current maximum of 5 A, but these data may be varied by the user as required.

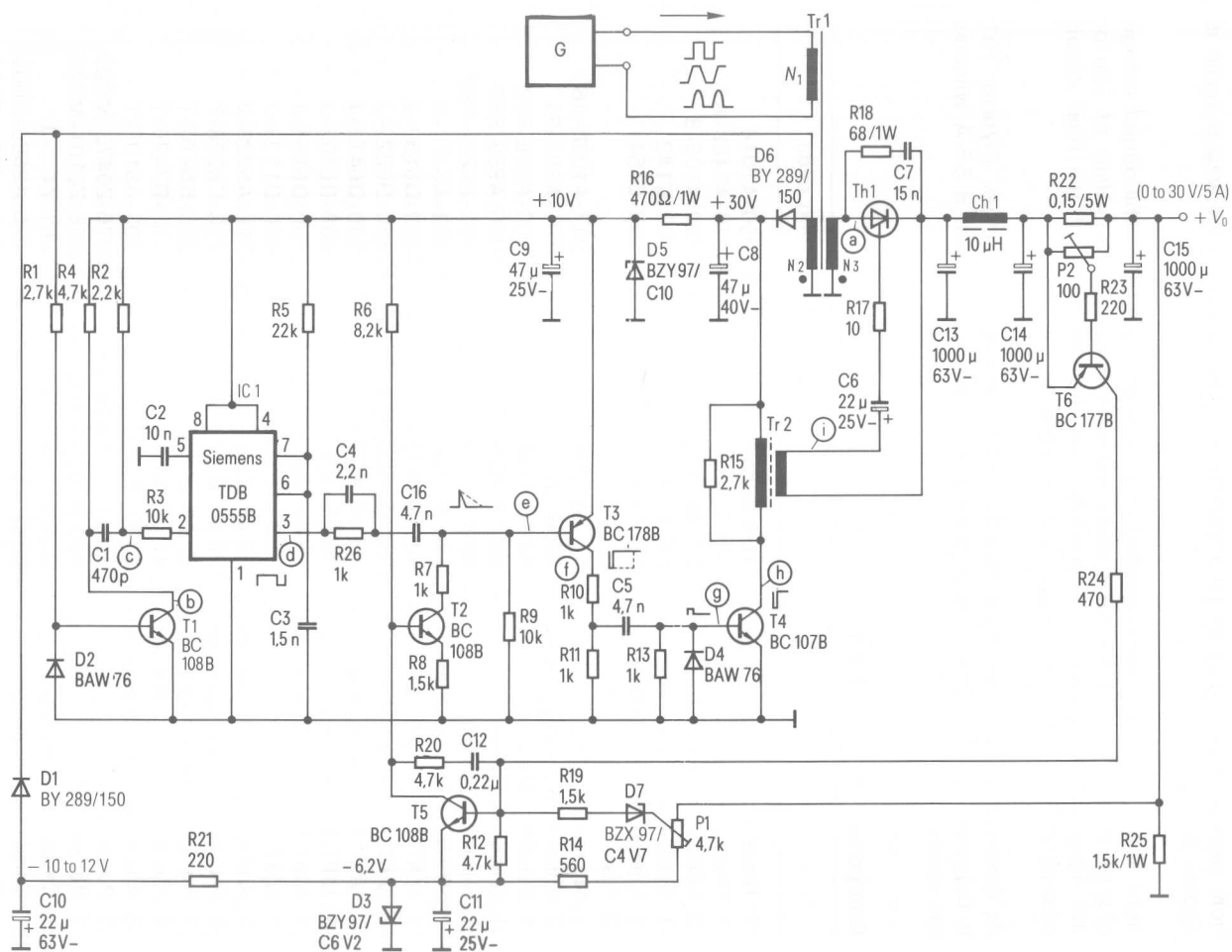
The external generator G supplies a half-sine-wave voltage to winding N_1 of transformer Tr1. The generator current is triangle-shaped.

The NPN-transistor T_1 is operated via R_1 by the ac voltage of the auxiliary winding N_2 . At positive zero crossing of this dc voltage, transistor T_1 becomes conductive and the differentiating circuit consisting of C_1 and R_2 is connected to ground. The IC TDB 0555B operates as a monostable multivibrator, i.e. H-level is applied to output 3. It is triggered by the negative edge of the pulse applied to pin 2 of IC1. The time constant $t = R_5 \times C_3$ is chosen in that the multivibrator will remain at H-level longer than the positive half-wave of the secondary voltage at winding N_3 .

The NPN-transistor T_2 is already conductive by a signal applied via R_6 . Resistors R_7 and R_8 as well as transistor T_2 are connected in series. Resistor R_9 is parallelly connected. Therefore the total resistance is low when transistor T_2 is conducting. In this case T_5 is switched off. The output pulses of IC1 are differentiated by C_4 , C_{16} and the resistor network consisting of R_7 (T_2), R_8 and R_9 . Transistor T_3 is blocked for 2 to 3 μ s after the positive edge of the signal is available at pin 3 of IC1. The voltage at point f is again differentiated by R_{13} and C_5 in that the driver transistor T_4 becomes conductive for 5 to 8 μ s. As soon as the desired output voltage being adjusted by potentiometer P_1 is reached, the controlling amplifier including T_5 gets conductive and supplies a negative reverse voltage of -6.2 V (Z-diode D_3) to transistor T_2 . Now transistor T_3 remains turned off for a longer period and the thyristor will be triggered later.

The longer transistor T_3 is turned off, i.e. the higher the positive deviation of the output voltage to be controlled, the later the collector voltage at f will jump

Fig. 8.5



from zero to +10 V to turn on transistor T_4 . The width of the trigger pulse is approx. 6 to 8 μ s.

Input voltage variations are controlled to a value of about 0.1%. The output voltage change is $\leq 1\%$ when the load varies between 0 and 100%. Values of 1‰ for the ripple are obtainable in dependence on the dimension of the filter circuit incorporating C_{13} , Ch1 and C_{14} .

At short-circuit operation transistors T_6 and T_5 become conductive. Thyristor Th1 is triggered later. The short-circuit current of the described circuit is 5.5 A whereas the nominal value is 5 A.

Components for circuit 8.5

		Ordering code
1 Timer IC	TDB 0555B	Q67000-A1044
1 Thyristor	BSt C 0606 (T0-66)	C66048-A1408-A2
3 Silicon-AF-transistors	BC 108B	Q62702-X108-B
1 Silicon-AF-transistor	BC 177B	Q62702-C142
1 Silicon-AF-transistor	BC 178B	Q62702-C154
2 Fast silicon rectifier diodes	BY 289/150	C66047-A1028-A8
2 Silicon-switching diodes	BAW 76	Q60201-A397-F4
1 Silicon-Z-Diode	BZY 97/C6V2, 1.5 W	Q68000-A948-F82
1 Silicon-Z-Diode	BZY 97/C10	Q68000-A953-F82
1 Silicon-Z-Diode	BZX 97/C4V7	Q62702-Z1227-F82
1 STYROFLEX-capacitor	470 pF, 63 V	B31063-A5471-H
1 MKT-layer capacitor	1.5 nF, 400 V	B32560-D6152-J
1 MKT-layer capacitor	2.2 nF, 400 V	B32560-D6222-J
2 MKT-layer capacitors	4.7 nF, 400 V	B32560-D6472-J
1 MKT-layer capacitor	10 nF, 400 V	B32560-D6103-J
1 MKT-layer capacitor	15 nF, 400 V	B32560-D6153-J
1 MKT-layer capacitor	0.22 μ F, 100 V	B32560-D1224-J
2 Alu-electrolytic capacitors	22 μ F, 25 V	B41313-A5226-V
1 Alu-electrolytic capacitor	22 μ F, 63 V	B41283-C8226-T
1 Alu-electrolytic capacitor	47 μ F, 25 V	B41283-B5476-T
1 Alu-electrolytic capacitor	47 μ F, 40 V	B41283-D7476-T
3 Alu-electrolytic capacitors	1000 μ F, 63 V	B41293-A8108-T
1 Potentiometer	4.7 k Ω , 0.2 W (vertical)	B58076-Z0472-M320
1 Potentiometer	100 Ω , 0.2 W (vertical)	B78076-Z0101-M320
21 Carbon film resistors	0.33 W, $\pm 5\%$	B51261-Z4...-J1
1 Carbon film resistor	68 Ω /1 W	B51276-A2680-G000
1 Carbon film resistor	470 Ω /1 W	B51276-A2471-G000
1 Carbon film resistor	1.5 k Ω /1 W	B51276-A2152-G000
1 Wire resistor consisting of 2 parallelly connected resistors 0.3 Ω /7 W	0.15 Ω /5 W	B52136-A000-K300
1 Choke with air gap	10 μ H/5 A	—

8.6 Switch Mode Power Supply with Variable Operating-Frequency

Special applications can be met with switch mode power supplies, the operating frequency of which are alternatively selectable. That means the operating current can be varied in dependence on a program by inductive or inductive/resistive loads. Inductive loads are contactors, magnetic clutches, relays etc. Therefore the starting current can be rated higher than the hold one to obtain very short pull-up times.

The generator circuit shown in **fig. 8.6.1** operates as astable multivibrator, however, the bases of T_1 and T_2 are controlled by an impressed current. These constant currents, being adjustable by potentiometers R_1 , R_2 and R_3 , are generated by transistors T_3 and T_4 . The frequency maximum is set by R_3 and the minimum by R_1 . A regulated voltage of 10 V is applied to the bases of T_3 and T_4 by means of z-diode D_1 . Thus the set frequency remains constant even if the voltage varies.

The possible maximum of the impressed current is adjusted by emitter resistors R_3 , R_4 and R_5 (f_{max}).

The constant-currents charge alternatively capacitors C_2 and C_3 . The discharge is released by switching transistors T_1 and T_2 . During the charging process the amplitude of the output signals being available at points A and B are rounded off a little bit.

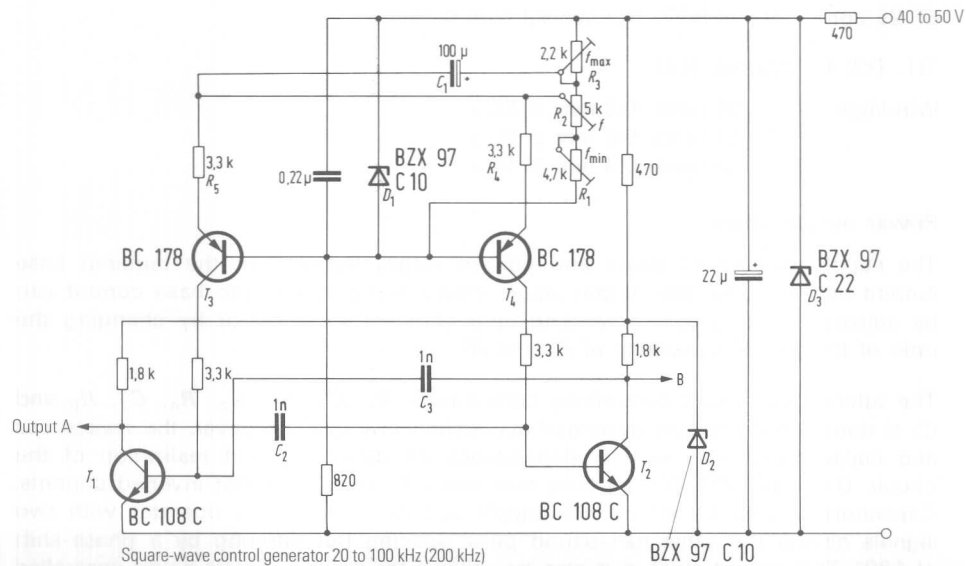


Fig. 8.6.1

The capacitance of C_1 influences the starting characteristic of the switch mode power supply and C_1 guarantees a start operation with a high frequency. This is very important for SMPSs. The described square-wave generator supplies a signal with a frequency being adjustable between 10 kHz and 200 kHz.

Variable-frequency square-wave generator with pulse separation processing and driver

Fig. 8.6.2 shows a simple variable-frequency multivibrator operating as control generator and using transistors T_1 and T'_1 . The achievable frequency variation is less than with the generator of circuit 8.6.1.

For push-pull operation the control currents have to operate with pulse separations because of transistor switching times and other delays. The required pulse spaces of the output signal are generated by means of the circuits comprising R_4 , C_4 , R'_4 , C'_4 , C_1 , C_2 , R_1 and R_2 . One pulse separation of the output signal is adjustable by R_2 (e.g. 4 μ s) and potentiometer R_3 is commonly responsible for all pulse spaces. The pulse separations are easily generated by charging capacitors C_1 , C_2 and C_3 in that a control of T_2 and T'_2 is only possible during the voltage peaks. The amplifying transistors T_2 and T'_2 process the signal in that two voltages, being shifted by half of a period, are generated as required for push-pull operation.

It should be mentioned that an adequate control generator with variable duty cycles can be alternatively connected to pins A and B (fig. 8.6.2). In this case the pulse space generation is already achieved by the control generator or can be obtained as already described.

Transistors T_3 and T_4 as well as T'_3 and T'_4 operate via C_2 in a series push-pull mode. They are connected to driver transformers Tr1 and Tr2 utilizing both an EF 25 core, material N27. The special core data are:

Tr1, Tr2: EF 25, mat. N27

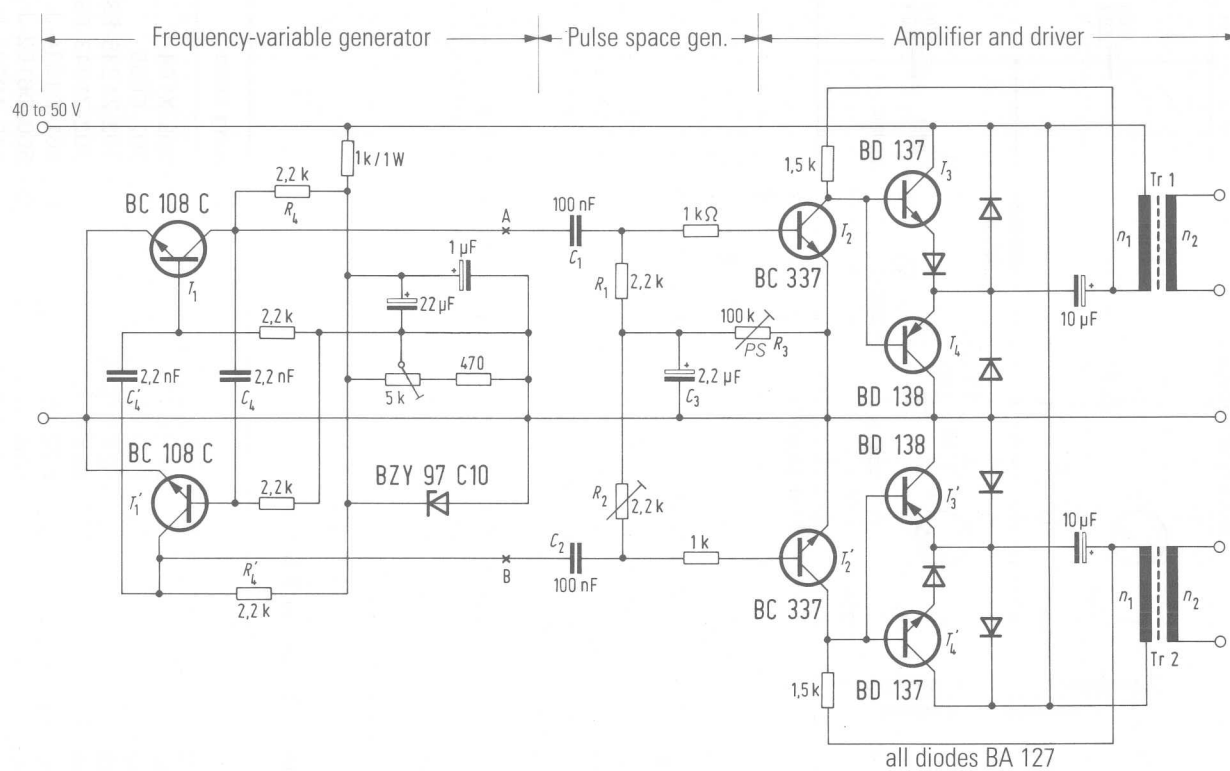
Windings 1–2: 50 turns, 0.3 mm $\varnothing$ ECu
 3–4: 18 turns, 0.6 mm $\varnothing$ ECu
 5–6: 50 turns, 0.3 mm $\varnothing$ ECu

Power output stage

The supply voltage of driver and control stage depends on the required base current maximum for the output stage shown in **fig. 8.6.3**. The base current can be adjusted by varying the winding ratio of transformer Tr1 or by changing the ratio of the divider consisting of R_2 and R'_2 .

The attenuating circuit comprising components R_1 , C_1 , R_3 , C_2 , R_4 , C_3 , R_5 and C_4 is dimensioned for the described application example. However, the resistances and capacitances may vary in dependence on dimension and realization of the circuit. Diode BY 294/400 protects transistors T_1 and T_2 against inverted currents. Capacitors C_6 and C_7 smooth the supply voltage if the device operates with two signals having the same half-period pulse spacing but differing by a phase-shift of 180°. This output stage can also be utilized for driving signals being controlled by frequency or by pulse separations.

Fig. 8.6.2



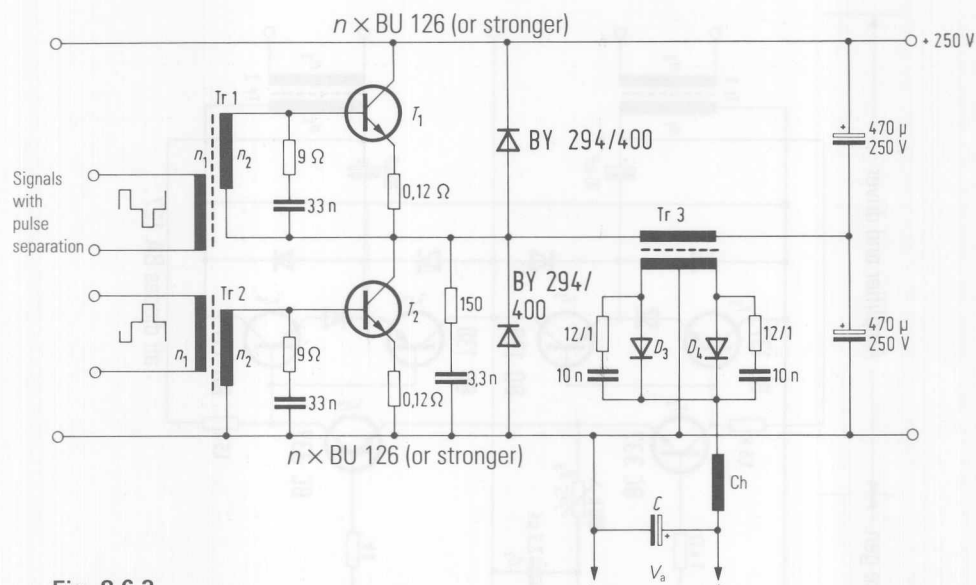


Fig. 8.6.3

Components for circuit 8.6.1

			Ordering code
2 Transistors	BC 108C		Q60203-X108-C
2 Transistors	BC 178		Q62702-C685
2 Z-diodes	BZX 97C10		Q62702-Z1235-F82
1 Z-diode	BZX 97C22		Q62702-Z1243-F82
1 MKT-capacitor	0.22 μF		B32561-D1224-J
2 MKT-capacitors	1 μF		B32560-D6102-J
1 Electrolytic capacitor	22 μF/63 V		B41316-A8226-V
1 Electrolytic capacitor	100 μF/25 V		B41316-A5107-V
2 Resistors	470 Ω/0.5 W		B51261-Z4471-J1
1 Resistor	820 Ω/0.5 W		B51261-Z4821-J1
2 Resistors	1.8 kΩ/0.5 W		B51261-Z4182-J1
4 Resistors	3.3 kΩ/0.5 W		B51261-Z4332-J1

Components for circuit 8.6.2

		Ordering code
2 Transistors	BC 108C	Q60203-X108-C
2 Transistors	BC 337	Q62702-C313
2 Transistors	BD 137	Q62702-D108
2 Transistors	BD 138	Q62702-D109
1 Z-diode	BZY 97C10	Q68000-A953-F82
6 Diodes	BA 127	Q60201-X127-D9
2 MKT-capacitors	2.2 nF	B32560-D6222-J
2 MKT-capacitors	100 nF	B32561-D3104-J
1 Electrolytic capacitor	1 μ F/63 V	B41316-A8105-V
1 Electrolytic capacitor	2.2 μ F/63 V	B41316-A8225-V
2 Electrolytic capacitors	10 μ F/63 V	B41316-A8106-V
1 Electrolytic capacitor	22 μ F/63 V	B41316-A7226-V
1 Resistor	470 Ω /0.5 W	B51261-Z4471-J1
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	1 k Ω /1 W	B51276-A2102-G
2 Resistors	1.5 k Ω /0.5 W	B51261-Z4152-J1
5 Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1

Components for circuit 8.6.3

		Ordering code
2 Transistors	BU 126	Q62702-U167
2 Diodes	BY 294/400	C66047-A1060-A7
1 MKT-capacitor	3.3 nF/400 V	B32560-D6332-J
2 MKT-capacitors	10 nF/400 V	B32560-D6103-J
2 MKT-capacitors	33 nF/250 V	B32561-D3333-J
2 Electrolytic capacitors	470 μ F/250 V	B43306-A2477-T
$Tr3 - Ch - D_3 - D_4 - C$ in accordance to the required secondary voltage		
2 Resistors	9 Ω /1 W	B51276-A2090-G100
2 Resistors	12 Ω /1 W	B51276-A2120-G
1 Resistor	150 Ω /0.5 W	B51261-Z4151-J1

8.7 Generator for Pulses with Spaces Required for Push-Pull Switch Mode Power Supplies

Push-Pull output stages of switch mode power supplies have to be operated by pulses having spaces between the pulses in accordance to the switching time of the used power transistors. Fig. 8.7.1 shows a circuit for this special application. The signal of the circuit including L , C_1 and C_2 is coupled to transistors T_1 and T_2 via capacitors C_3 and C_4 . As the transistors become only conductive during the peaks of the sine signal a staircase signal is available at the transistor outputs (see fig. 8.7.2). The bases of transistors T_3 and T_4 are connected to the collectors of T_1 and T_2 , both operating as common emitter-circuit and being alternatively triggered.

Transistors T_1 and T_2 are not conductive during the pulse spaces. A voltage being divided to half of the supply voltage by resistors R_2 and R_3 is applied to base of T_3 and T_4 . Its output signal is supplied via C_5 to transformer Tr. The latter has an attenuation effect when the magnetic energy changes its polarity. Therefore the staircase output voltage only shows a few overshoots.

The total circuit operates in accordance to the principle of a self-oscillating generator with fixed frequency. The output voltage of the common-emitter circuit is feedbacked via resistor R_4 to the L/C_2 -circuit. The correct phase is achieved by the two single capacitors C_1 and C_2 .

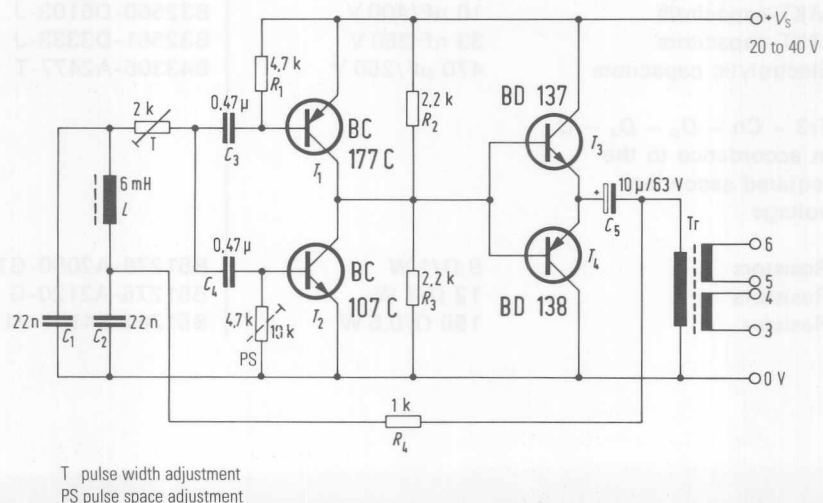


Fig. 8.7.1

The circuit automatically starts to oscillate when the supply voltage is applied, as T_3 is conductive and thus capacitor C_5 is charged. A current delayed by R_4 , L and C_4 flows to the base of T_2 and generates the oscillation. At steady-state conditions all transistors operate as switches. The inductor is realized by a coil wound on a boot-shaped core with the dimensions of $20\text{ mm} \times 6\text{ mm } \varnothing$ and with winding as shown in the schematic of **fig. 8.7.3**.

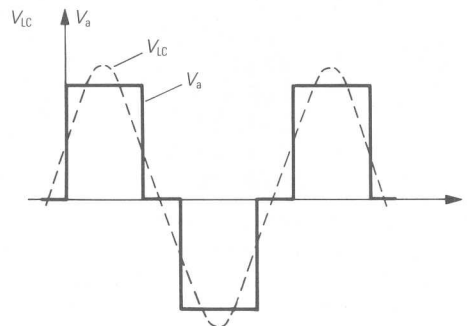


Fig. 8.7.2

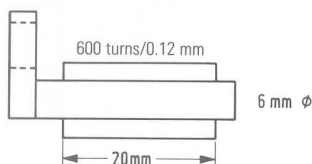


Fig. 8.7.3

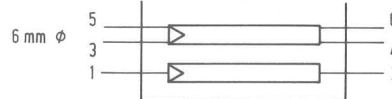


Fig. 8.7.4

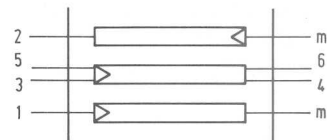


Fig. 8.7.5

L : boot-shaped $20 \times 6\text{ mm } \varnothing$, screw core $16 \times 4.5\text{ mm } \varnothing$
 $n = 600$ turns 0.12 ECU , without layer insulation

For the transformer the following two examples are given in accordance to **fig. 8.7.4** and **fig. 8.7.5**.

EF 20 N27 without air gap

Winding 1–2: 100 turns/ 0.2 ECU
 3–4: 8 turns/ 0.4 ECU silk } double wound } for 0.5 to 2 A_{sec}
 5–6: 8 turns/ 0.4 ECU silk }

(fig. 8.7.4)

EF 25 N27 A 630

Winding 1–m: 50 turns/ 0.3 ECU
 3–4: 12 turns/ 0.5 ECU silk } double wound } for 2 to 5 A_{sec}
 5–6: 12 turns/ 0.5 ECU silk }
 m–2: 50 turns/ 0.3 ECU

(fig. 8.7.5)

Components for circuit 8.7.1

			Ordering code
1	Transistor	BC 107C	Q60203-X107-C
1	Transistor	BC 177C	Q62702-C143
1	Transistor	BD 137	Q62702-D108
1	Transistor	BD 138	Q62702-D109
2	MKT-layer capacitors	22 nF/250 V	B32510-D3223-K
2	MKT-layer capacitors	0.47 μ F/100 V	B32512-D1474-K
1	Electrolytic capacitor	10 μ F/63 V	B41238-A8106-T
2	Resistors	2.2 k Ω /0.5 W	B51261-Z4222-J1
1	Resistor	4.7 k Ω /0.5 W	B51261-Z4472-J1
2	Pot cores	EF 20d N27	B66317-G100-X127

8.8 DC-Converter for 50 Watt Using SIPMOS-Power-Transistors and Control IC TDA 4700

The described converter operates as a push-pull circuit. It utilizes the control IC TDA 4700 which supplies the necessary signals for all control and regulating functions, whereby a minimum of external components is required. The circuit is specified for input voltages between 20 and 28 V. The output voltage is 5 V at a maximum current of 10 A. The oscillation frequency of the IC is 40 kHz. Input and output are not isolated. The output signals of the TDA 4700 are pulse-width-modulated. They control via a push-pull circuit the gate of the SIPMOS-transistors, whereby a small control power is only dissipated. The source currents are applied via common resistor R_8 , operating as sensor for a dynamic current limitation by utilizing its voltage drop. Thus the converter is protected against short-circuit operation.

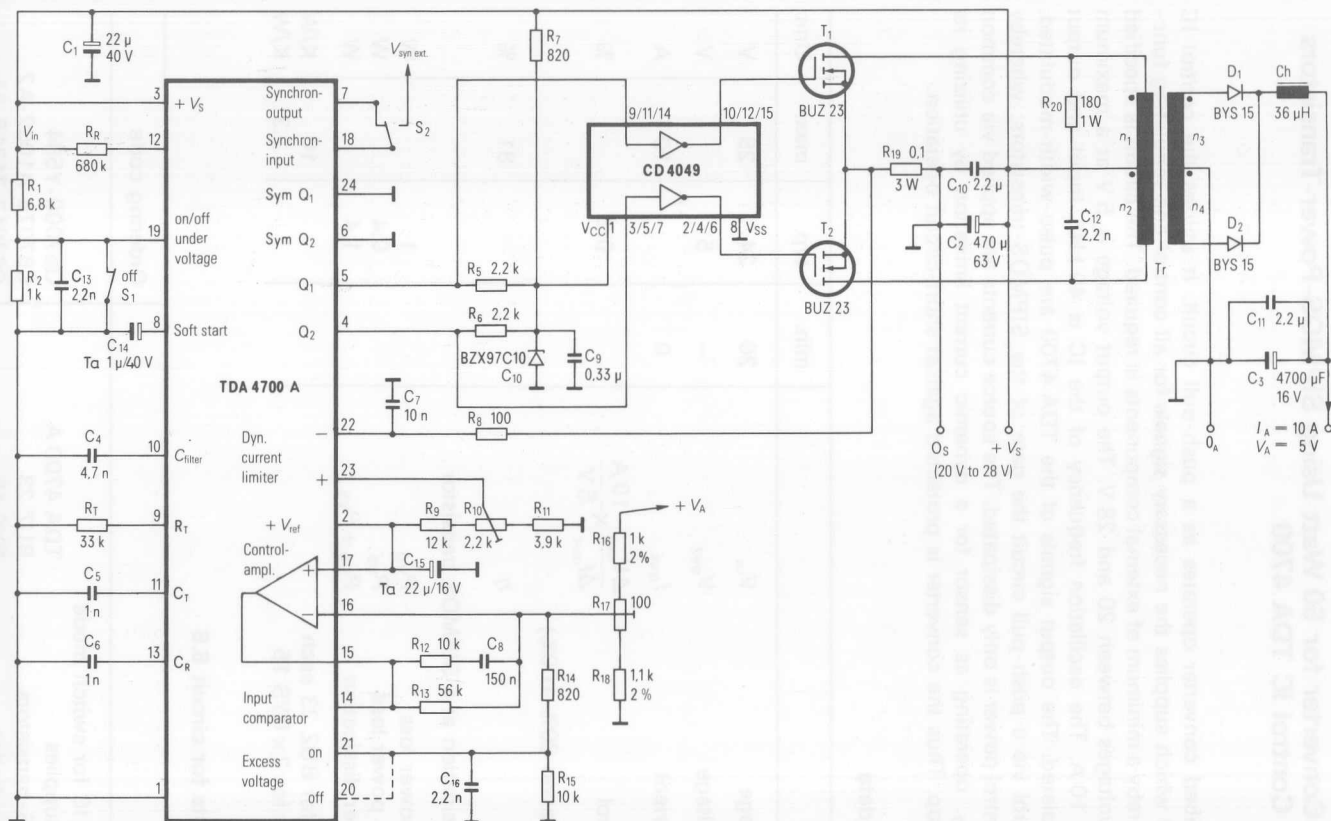
Technical data

		min.	typ.	max.	Unit
Input voltage	V_{in}	20	24	28	V
Output voltage	V_{out}	—	5		V
Output current	I_{out}	0		10	A
Load control	$\frac{\Delta V_{out}}{\Delta I_{out}} \times \frac{10 \text{ A}}{5 \text{ V}}$		0.2		%
(Load variation 30%–100%)					
Efficiency	η			81	%
Power dissipation at a SIPMOS transistor					
Forward power loss	P_{VD}		1		W
Switching power loss	P_{VS}		0.4		W
Total power dissipation	$P_{VD} + P_{VS}$		1.4		W
Heat sink for BUZ 23 each				10	K/W
Heat sinks for 2 × BYS 15				2.3	K/W

Components for circuit 8.8

		Ordering code
1 Control IC for switch mode power supplies	TDA 4700 A	Q67000-Y594
2 SIPMOS-transistors	BUZ 23	C67078-A1002-A2
2 Schottky-diodes	BYS 15	C67017-Z1318-A1
1 Z-diode	BZX 97 C 10	Q62702-Z1235-F82
1 CMOS-inverter	CD 4049	—

Fig. 8.8
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Components for circuit 8.8 (continued)

		Ordering code
1 Potentiometer	100Ω	B51655-Z101-M401
1 Potentiometer	2.2 kΩ	B58655-Z222-M401
2 MKT-layer capacitors	1 nF/400 V	B32560-D6102-J
3 MKT-layer capacitors	2.2 nF/400 V	B32560-D6222-K
1 MKT-layer capacitor	4.7 nF/400 V	B32560-D6472-K
1 MKT-layer capacitor	0.01 μF/400 V	B32560-D6103-K
1 MKT-layer capacitor	0.15 μF/100 V	B32560-D1154-K
1 MKT-layer capacitor	0.33 μF/100 V	B32560-D1334-J
2 MKT-layer capacitors	2.2 μF/100 V	B32562-D1225-K
1 Ta-electrolytic capacitor	1 μF/40 V	B45181-C4105-M
1 Ta-electrolytic capacitor	22 μF/16 V	B45181-B2226-M
1 Al-electrolytic capacitor	22 μF/40 V	B41316-A7226-V
1 Al-electrolytic capacitor	470 μF/63 V	B41010-D8477-T
1 Al-electrolytic capacitor	4700 μF/16 V	B41010-C4478-T
1 Resistor	0.1 Ω/3 W	—
1 Resistor	100 Ω/0.5 W	B51560-Z4101-J1
1 Resistor	180 Ω/1 W	B54314-Z5181-G1
2 Resistors	820 Ω/0.5 W	B51261-Z4821-J1
1 Resistor	1 kΩ/0.5 W	B51260-Z4102-J1
1 Resistor	1 kΩ/0.5 W 2%	B51261-Z4102-G1
2 Resistors	2.2 kΩ/0.5 W	B51260-Z4222-J1
1 Resistor	6.8 kΩ/0.5 W	B51260-Z4682-J1
1 Resistor	10 kΩ/0.5 W	B51260-Z4103-J1
1 Resistor	1.1 kΩ/0.5 W 1%	B54310-Z5112-F2
1 Resistor	12 kΩ/0.5 W	B51260-Z4133-J1
1 Resistor	33 kΩ/0.5 W	B51260-Z4333-J1
1 Resistor	39 kΩ/0.5 W	B51260-Z4393-J1
1 Resistor	56 kΩ/0.5 W	B51260-Z4563-J1
1 Resistor	680 kΩ/0.5 W	B51276-A2684-G
1 Switch	S1	C42315-A60-A1
Transformer Tr		
1 core EC41, N27, without air gap		B66339-G0000-X127
1 Coil former		B66274-A1001-T001
1 Assembly		B66274-B2001-X000
Windings: prim. $n_1 = n_2 = 14$ turns. bifilar, litz 120 × 0, 1 ESSCu sec. $n_3 = n_4 = 5$ turns bifilar, litz 120 × 0.1 ESSCu		
Choke Ch		
1 Core RM12, N41, $A_L = 160$		B65815-J0160-A041
1 Coil former		B65816-A1002-D001
2 Clamps		B65816-A2001-X000
Winding: 15 turns, litz 100 × 0.1 ECu		

9. Microcomputer Applications with SAB 8080 and SAB 8085

9.1 Keyboard-IC S 600/8255 in Conjunction with 8-bit Microprocessors

Introduction

With the IC S 600 it is possible to operate a keyboard of 10×9 push buttons and 10 control keys. It supplies in parallel a 10-bit information corresponding to the operated push button.

As a total number of 360 bit-patterns can be stored this IC is suited to operate as encoder for larger keyboards. The S 600 can also be utilized as input of an 8-bit microcomputer. The application of the keyboard IC is demonstrated in conjunction with "Mikroset 8080".

Input via I/O peripheral interface SAB 8255

The information is transferred from the slow operating P-MOS-IC S 600 to the fast reacting microcomputer system without any problems, as the data is intermediately stored by the I/O peripheral interface SAB 8255 of the Mikroset 8080. S 600 is connected to port A since port B and three lines of port C ($PC_{0,1,2}$) are internally required by the Mikroset 8080. Besides that $PC_{3,4,5}$ are utilized for the acknowledgement procedure between S 600 and SAB 8255 and for interrupt request.

This solution is always convenient when a system incorporates already an SAB 8255 for other purposes and when this I/O peripheral interface does not utilize one of the 8-bit ports and 3 lines of port C.

The circuit is shown in **fig. 9.1.1**.

From the 10-bit-pattern offered by the S 600 only the lower 8 bits are utilized and directly supplied to pins PA_0 to PA_7 of the SAB 8255. The acknowledgement signal with active-LOW is directly applied from the S 600 to input PC_4 of SAB 8255. However, the acknowledgement signal with active-HIGH at PC_5 has to be inverted before it is supplied back to S 600. The interrupt request, available at PC_3 of the SAB 8255, has also to be inverted since the Mikroset 8080-bus requires an $\overline{INT}$ -signal, i.e. active-LOW. For releasing an interrupt request of the SAB 8255 the enable flip-flop $INTE_A$ of SAB 8255 has to be set by a programmed bit-setting of PC_4 .

A simple program example is "S 600/8255" as shown in **fig. 9.1.2**. In the main program the I/O peripheral interface SAB 8255 is set to mode 1 (strobed input/output) by control word 0B7H after the interrupt request is enabled. In this case the hexadecimal figure B is only relevant. Figure 7 is of no importance as pins PC_6 and PC_7 are not required and as port B is internally utilized, that means it is not at the user's disposal. Then the control word 39H is supplied to the same address. It includes the leading zero (hexadecimal figure 3) and the second

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('S600/8255')
		2	;HAUPTPROGRAMM
0700		3	ORG 0700H
0700 FB		4	EI ;INTERRUPTFREIGABE
0701 3EB7		5	MVI A,0B7H ;STEUERWORT FUER I/C+PORT
0703 D3FF		6	OUT 0FFH ;AUSGEBEN AN 8255
0705 3E39		7	MVI A,39H ;STEUERWORT FUER C4
0707 D3FF		8	OUT 0FFH ;AUSGEBEN AN 8255
0709 210000		9	LXI H,00H ;HL NULLSETZEN
070C 5C		10	MOV E,H ;E NULLSETZEN (ZAEHLT INTERRUPTS)
070D CDC001		11	ANZE: CALL 01C0H ;ANZEIGE DER DATEN *)
0710 7B		12	MOV A,E ;INTERRUPTZAEHLER NACH A
0711 CDD301		13	CALL 01D3H ;ANZEIGE DER ANSCHLAEGE **)
0714 C30D07		14	JMP ANZE ;
07FA		15	ORG 07FAH
07FA C32007		16	JMP 0720H ;STARTADRESSE FUER INTERRUPTROUTINE
		17	;INTERRUPTPROGRAMM
0720		18	ORG 0720H
0720 29		19	DAD H ;
0721 29		20	DAD H ;)HL-WORT UM EIN ZEICHEN
0722 29		21	DAD H ;)NACH LINKS
0723 29		22	DAD H ;
0724 DBFC		23	IN 0FCH ;EINLESEN
0726 0F		24	RRC ;
0727 0F		25	RRC ;)LINKE HEXZIFFER
0728 0F		26	RRC ;)NACH RECHTS
0729 0F		27	RRC ;
072A E60F		28	ANI 0FH ;MASKIERUNG
072C B5		29	ORA L ;UEBERSCHREIBUNG IM AKKU
072D 6F		30	MOV L,A ;ZURUECK NACH L
072E 13		31	INX D ;DE UM EINS HOEHER ZAEHLEN
072F FB		32	EI ;INTERRUPTFREIGABE
0730 C9		33	RET ;RUECKSPRUNG
		34	END

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS
ANZE A 070D

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.1.2

hexadecimal figure 9 which sets the internal interrupt enable flip-flop of the SAB 8255. The control word address of the Mikroset 8080 is 0FFH.

After setting the required registers to zero, the main program is finished with a loop which displays the register pair H, L on the 4-digit address display. Register E is shown on the 2-digit data display of the Mikroset 8080.

The SAB 8080 always jumps to the interrupt routine when one of the push buttons of the S 600 is operated.

As demonstration example a special program was chosen. It utilizes only the upper four bits of the 8-bit information of the S 600 and writes the corresponding hexadeci-

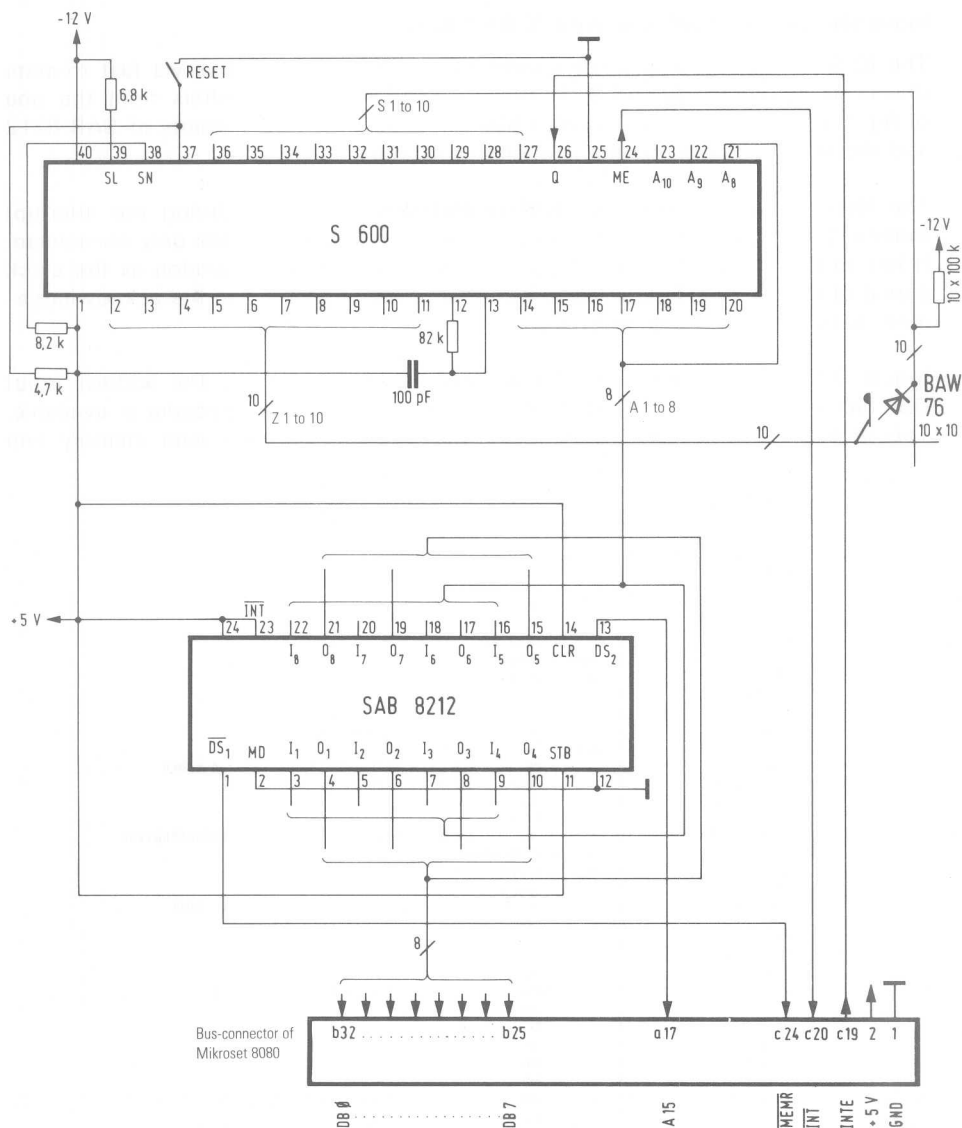


Fig. 9.1.3

mal figure at the last digit of the address (register pair H, L). The previously loaded figures are shifted to left by one digit. The older figure, being previously in the upper part of register H, is shifted out and is lost. Register E adds all push button operations and when 0FFH is reached it starts again at 00.

Input via the SAB 8080-bus with IC SAB 8212

The IC S 600 is advantageously connected to the SAB 8080-bus via fast tri-state drivers as shown in **fig. 9.1.3**. In this case the circuit only differs from the one of fig. 9.1.1 in that the outputs of S 600 are connected to the inputs of SAB 8212 and the acknowledgement line is directly connected to the bus.

The INTE-signal is utilized for acknowledgement. It is low during the interrupt routine. This is applicable, if interrupt requests for data transfer are only considered. It has to be assured that the interrupt routine has the same duration as the clock period of the S 600 (15 µs). If it is less, then it may happen that the acknowledgement is not always accepted by the S 600.

Inputs $\overline{DS}_1$ and DS_2 are suited for addressing the SAB 8212. The address input $\overline{DS}_1$ has to be connected to $\overline{MEM R}$, if no additional address decoder is available. This measure is necessary as both the I/O-write line and the read memory line

ASM80 S600B.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0
S600/8212

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	\$TITLE('S600/8212')
		2	;HAUPTPROGRAMM
		3	ORG 0700H
0700		4	EI ;
0700 FB		5	LXI H,0000H ;HL NULLSETZEN
0704 5C		6	MOV E,H ;E NULLSETZEN
0705 CDC001		7	ANZA: CALL 01C0H ;ANZEIGE DER DATEN
0708 5F		8	MOV E,A ;INTERRUPTZAEHLER NACH A LADEN
0709 CDD301		9	CALL 01D3H ;ANZEIGE DER ANSCHLAEGE
070C C30507		10	JMP ANZA ;
07FA		11	ORG 07FAH
07FA C32007		12	JMP 0720H ;STARTADRESSE FUER INTERRUPTROUTINE
		13	;INTERRUPTPROGRAMM
0720		14	ORG 0720H
0720 29		15	DAD H ;
0721 29		16	DAD H ;)HL/WORT UM 4 BIT NACH LINKS
0722 29		17	DAD H ;
0723 29		18	DAD H ;
0724 3A0000		19	LDA 0000H ;EINLESEN AUS TASTATUR
0727 0F		20	RRC ;
0728 0F		21	RRC ;)AKKU 4 BIT NACH RECHTS
0729 0F		22	RRC ;
072A 0F		23	RRC ;
072B E60F		24	ANI 0FH ;MASKIEREN
072D B5		25	ORA L ;UEBERSCHREIBEN
072E 6F		26	MOV L,A ;ZURUECK NACH L
072F 13		27	INX D ;DE UM 1 HOEHER ZAEHLEN
0730 FB		28	EI ;INTERRUPTFREIGABE
0731 C9		29	RET ;RUECKSPRUNG
		30	END

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS

ANZA A 0705

ASSEMBLY COMPLETE, NO ERRORS

Fig. 9.1.4

Note: For translation of the German comments pls. see preceding text.

of the Mikroset 8080 have an active-LOW signal. The individual addressing is realized by input DS₂ with active-HIGH level.

As all I/O-address bits with active-HIGH are already utilized in the Mikroset 8080 (FC to FF) the described example "memory mapped" was chosen. In this case the address bit A₁₅ is used for addressing the keyboard (addresses 8000 to FFFF).

The program "S 600/8212", the listing of which is shown in **fig. 9.1.4**, offers the same functions as the "S 600/8255/S 600/8212". But the SAB 8212-outputs are connected to the 8080-system-bus.

Components for circuit 9.1.1

		Ordering code
1 Keyboard encoder with intermediate memory	S 600 E5-T	Q67100-Z133-V5
4 NAND-gates	7400	Q67000-H1
1 LED	LD 37 A	Q67703-Q99-S1
11 Diodes	BAW 76	Q62702-A397
1 Polypropylene-capacitor	100 pF/630 V	B33063-B6101-H
1 Resistor	330 Ω/0.5 W	B51261-Z4331-J1
1 Resistor	1 kΩ/0.5 W	B51261-Z4102-J1
1 Resistor	4.7 kΩ/0.5 W	B51261-Z4472-J1
1 Resistor	6.8 kΩ/0.5 W	B51261-Z4682-J1
1 Resistor	8.2 kΩ/0.5 W	B51261-Z4822-J1
10 Resistors	10 kΩ/0.5 W	B51261-Z4103-J1
1 Resistor	82 kΩ/0.5 W	B51261-Z4823-J1
additional for circuit 9.1.3		
1 Resistor	4.7 kΩ/0.5 W	B51261-Z4472-J1
1 Resistor	6.8 kΩ/0.5 W	B51261-Z4682-J1
1 Resistor	8.2 kΩ/0.5 W	B51261-Z4822-J1
1 Resistor	82 kΩ/0.5 W	B51261-Z4823-J1
10 Resistors	100 kΩ/0.5 W	B51261-Z4104-J1

9.2 Program for Indicating Duty Cycle of Pulse Trains

Electronic circuits for sensors very often supply a square wave signal, the duty cycle of which is a function of the measured mechanical or physical quantity. The following program is suited to indicate the pulse duty factor on the Mikroset 8080 display. It shows the ratio between pulse length (H-duration) and pulse repetition period (pulse interval).

The program averages the duty cycle over 16 intervals, divides the time for the pulse length by the one for the pulse interval, calculates the percentage and converts the hexadecimal number to a decimal one.

The described program is applicable to all 8080/8085-systems, if the address range is accordingly modified. The input signal with TTL-level is applied to PC₇ of the Mikroset 8080. For the single-chip microcomputer SAB 8048 a new program code and a new loop counter program have to be established.

Program

The program has a main part and 6 subroutines. The structogram is shown in fig. 9.2.1. The subroutines can also be called by other main programs for other purposes.

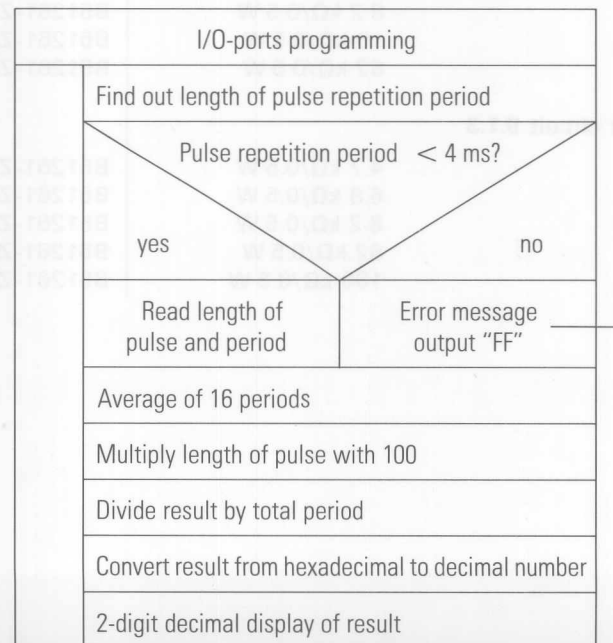


Fig. 9.2.1

Program "Sensor Auswertung" (sensor evaluation)

If a Mikroset 8080 is utilized the program being listed in **fig. 9.2.2** starts at address 0600H. First the I/O peripheral interface SAB 8255 is programmed in that pin PC₇ operates as input. The listing for subroutine "Test für Impulswiederholungsfrequenz" (pulse repetition frequency) is shown in **fig. 9.2.3**. It checks as to whether the pulse interval is not longer than 4 ms. A longer interval would cause an overflow of the counting register B. When a too low frequency is applied, i.e. interval >4 ms, an error message is displayed.

ASM80 SENSOR.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0
SENSOR-AUSWERTUNG

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('SENSOR-AUSWERTUNG')
		2	;FUNKTION:DAS PROGRAMM Liest DAS TASTVERHAELTNIS
		3	;EINES RECHTECKWECHSELS EIN,MITTELT UEBER 16 PERIODEN
		4	;BILDET DEN QUOTIENTEN DER H-TASTZEIT ZUR GESAMTLAENGE UND
		5	;GIBT DEN WERT IN PROZENTEN AUS.UEBERSCHREITET DIE PERIODEN-
		6	;LAENGE DIE OBERE MESSGRENZE VON 4 MS ERFOLGTE FEHLERMELDUNG FFFF
		7	;PROGRAMM ABLAUFFAEBIG AUF MIKROSET. EINGANG: PC7
		8	;MESSWERTUEBERGABE UEBER REGISTERPAAR H,L MIT ADRESSANZEIGE
0600		9	ORG 0600H
01C0		10	AANZ EQU 01C0H
0750		11	SPEICH EQU 0750H
00FE		12	PORTC EQU 0FEH
0776		13	ZELLE EQU SPEICH + 26H
		14	PUBLIC SPEICH
		15	PUBLIC ZELLE
		16	PUBLIC FEHL
		17	EXTRN TEST
		18	EXTRN TASTV
		19	EXTRN MITW
		20	EXTRN MUL100
		21	EXTRN DIVID
		22	EXTRN HEXBCD
		23	CSEG
0000 3E8A		24	START: MVI A,8AH ;
0002 D3FF		25	OUT 0FFH ;
0004 CD0000	E	26	CALL TEST
0007 CD0000	E	27	CALL TASTV
000A 215007		28	LXI H,SPEICH
000D CD0000	E	29	CALL MITW
0010 215107		30	LXI H,SPEICH+1
0013 CD0000	E	31	CALL MITW
0016 CD0000	E	32	CALL MUL100
0019 54		33	MOV D,H
001A 5D		34	MOV E,L
001B 217007		35	LXI H,SPEICH+20H
001E 6E		36	MOV L,M
001F 2600		37	MVI H,00
0021 AF		38	XRA A
0022 327607		39	STA ZELLE
0025 CD0000	E	40	CALL DIVID
0028 217607		41	LXI H,ZELLE
002B CD0000	E	42	CALL HEXBCD
002E 217607		43	LXI H,ZELLE
0031 5E		44	MOV E,M
0032 23		45	INX H
0033 AF		46	XRA A
0034 7E		47	MOV A,H
0035 17		48	RAL
0036 17		49	RAL
0037 17		50	RAL
0038 17		51	RAL
0039 B3		52	ORA E

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.2 (Page 1)

```

LOC  OBJ      SEQ      SOURCE STATEMENT
003A  5F      53      MOV      E,A
003B  23      54      INX      H
003C  56      55      MOV      D,M
003D  EB      56      XCHG
003E  CDC001  57      CALL     AANZ
0041  C30000  C 58      JMP      START
                    59
0044  26FF      60 FEHL:  MVI      H,0FFH
0046  2EFF      61      MVI      L,0FFH
0048  CDC001  62      CALL     AANZ
004B  C9      63      RET
                    64      END

PUBLIC SYMBOLS
FEHL  C 0044  SPEICH A 0750  ZELLE A 0776

EXTERNAL SYMBOLS
DIVID E 0000  HEXBCD E 0000  MITW  E 0000  MUL100 E 0000  TASTV  E 0000  TEST  E 0000

USER SYMBOLS
AANZ  A 01C0  DIVID E 0000  FEHL  C 0044  HEXBCD E 0000  MITW  E 0000  MUL100 E 0000  PORTC A 00FE
SPEICH A 0750  START C 0000  TASTV E 0000  TEST  E 0000  ZELLE A 0776

ASSEMBLY COMPLETE, NO ERRORS

```

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.2 (Page 2)

The next program is the subroutine "Tastverhältnis" (duty cycle). It reads 16 times the pulse length and loads it to the odd memory places and the pulse interval to the even ones. If a Mikroset 8080 is utilized the start-address of the memory is 0750H. Program "average" takes the average from these 16 measurements. Then the mean value for the pulse length is multiplied by 100 (decimal) and the subroutine "division" divides these pulse lengths, multiplied by 100, by the time of total pulse repetition period. By the multiplication with 100 the results are already indicated as percentage. The conversion from hexadecimal to decimal is realized by subroutine "hexadecimal-decimal-conversion". The corresponding BCD-number is located in three memory bytes of the RAM. Only two of them are required for an indication of up to 99%. But the first digit is also transferred to make the program more universal.

The main program packs the 3-digit number, covering 3 bytes, into 2 bytes and transfers them to the display of the Mikroset 8080.

When an error occurs register pair H, L is loaded with the hexadecimal number FFH and indicated on the address display.

The listing is shown in fig. 9.2.2. For better understanding the function of subroutine "Tastverhältnis" (duty cycle) is explained since the necessity of subroutine "test" is derived from it.

Subroutine "Tastverhältnis" (duty cycle)

First register pair H, L is loaded with the start address of the memory range as shown in the listing of fig. 9.2.4. Register D serves as loop counter for the

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('TEST FUER IMPULSWIEDERHOLUNGSFREQUENZ')
		2	;FUNKTION:DIE DAUER ZWEIER AUF EINANDERFOLGENDER H- UND L-SIGNALE
		3	;WIRD GETESTET. ERGIBT SICH EINE ZU LANGE ZEIT (KLEINE FREQUENZ),
		4	;DIE BEIM PROGRAMM 'TASTVERHAELTNIS' EINEN UEBERLAUF DES REGISTERS
		5	;ERGEBEN WUERDE, WIRD EINE FEHLERMELDUNG AUSGEGEREN.
		6	
		7	PUBLIC TEST
		8	EXTRN FEHL
00FE		9	PORTC EQU 0FEH
		10	CSEG
0000 0600		11	TEST: MVI B,0 ;
0002 DBFE		12	TEST1: IN PORTC ;
0004 E600		13	ANI 00H ;
0006 C20200 C		14	JNZ TEST1 ;
0009 DBFE		15	TEST2: IN PORTC ;
000B E600		16	ANI 00H ;
000D CA0900 C		17	JZ TEST2 ;
0010 3E01		18	TEST3: MVI A,01 ;
0012 00		19	ADD B ;
0013 DA0000 E		20	JC FEHL ;
0016 47		21	MOV B,A ;
0017 DBFE		22	IN PORTC ;
0019 E600		23	ANI 00H ;
001B C21000 C		24	JNZ TEST3 ;
001E 3E01		25	TEST4: MVI A,01 ;
0020 00		26	ADD B ;
0021 DA0000 E		27	JC FEHL ;
0024 47		28	MOV B,A ;
0025 DBFE		29	IN PORTC ;
0027 E600		30	ANI 00H ;
0029 CA1E00 C		31	JZ TEST4 ;
002C 78		32	MOV A,B ;
002D D69B		33	SUI 9BH ;
002F D20000 E		34	JNC FEHL ;
0032 C9		35	RET ;
		36	END ;

PUBLIC SYMBOLS
TEST C 0000

EXTERNAL SYMBOLS
FEHL E 0000

USER SYMBOLS
FEHL E 0000 PORTC A 00FE TEST C 0000 TEST1 C 0002 TEST2 C 0009 TEST3 C 0010 TEST4 C 001E

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.3

16 measurements. Register B takes the pulse repetition period and register C is loaded with the pulse length.

Two strobing loops with symbolic addresses ABF 1 and ABF 2 have been provided for forcing a defined start for counting pulse length (H-duration) and pulse repetition period (L-interval). Loop ABF 1 is not left as long as a signal with H-level is applied to PC₇. Then the program continues to loop ABF 2 as long as a signal with L-level is applied to PC₇ as shown in **fig. 9.2.5**.

When the level changes now from L to H, loop ABF 2 is left and the content of register D is incremented. The input value at PC₇ is strobed every 15.625 µs

LOC OBJ SEQ SOURCE STATEMENT

```

1 %TITLE('TASTVERHAELTNIS')
2 ;FUNKTION:AN KLEMMEN PC7 WIRD GEPRUEFT,WIE LANGE JEWEILS
3 ;H- ODER L-SIGNAL ANLIEGT.DIE LAENGE DES SIGNALS IST
4 ;PROPORTIONAL DER ANZAHL DURCHLAUFENER SCHLEIFEN,DIE
5 ;IN REGISTER B UND C EINGEZAHLT WERDEN.ZUR MITTELUNG
6 ;WERDEN 16 MESSUNGEN DURCHGEFUEHRT.DIE ZAHLEN FUER DIE
7 ;LAENGE DER H-SIGNALE WERDEN IN DEN UNGERADEN SPEICHER-
8 ;STELLEN,DIE ZAHLEN FUER DIE GESAMTLAENGE IN DEN GERADEN
9 ;SPEICHERSTELLEN UEBERGEHEN.
10 PUBLIC TASTV
11 EXTRN SPEICH
12 PORTC EQU 0FEH
13 CSEG
14 TASTV: LXI H,SPEICH;
15 MVI D,0 ;
16 ABF0: MVI B,0 ;
17 MVI C,0 ;
18 ABF1: IN PORTC ;
19 ANI 80H ;
20 JNZ ABF1 ;
21 ABF2: IN PORTC ;
22 ANI 80H ;
23 JZ ABF2 ;
24 INR D ;
25 ABF3: IN PORTC ;
26 INR B ;
27 ANI 80H ;
28 JNZ ABF3 ;
29 MOV C,B ;
30 ABF4: IN PORTC ;
31 INR B ;
32 ANI 80H ;
33 JZ ABF4 ;
34 MOV H,B ;
35 INX H ;
36 MOV H,C ;
37 INX H ;
38 MOV A,D ;
39 CPI 10H ;
40 JNZ ABF0 ;
41 RET ;
42 END

```

PUBLIC SYMBOLS

TASTV C 0000

EXTERNAL SYMBOLS

SPEICH E 0000

USER SYMBOLS

ABF0 C 0005 ABF1 C 0009 ABF2 C 0010 ABF3 C 0018 ABF4 C 0021 PORTC A 00FE SPEICH E 0000
TASTV C 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.4

by loop ABF 3. The content of register B is incremented after every strobe. When the level changes from H to L, the loop ABF 3 is left and the number of strobes is transferred from register B to C.

Now PC₇ is strobed every 15.625 µs by loop ABF 4. The number of strobes is added to the content of register B. Loop ABF 4 is left when the signal changes from L to H-level and the content of register B is loaded to the memory byte,

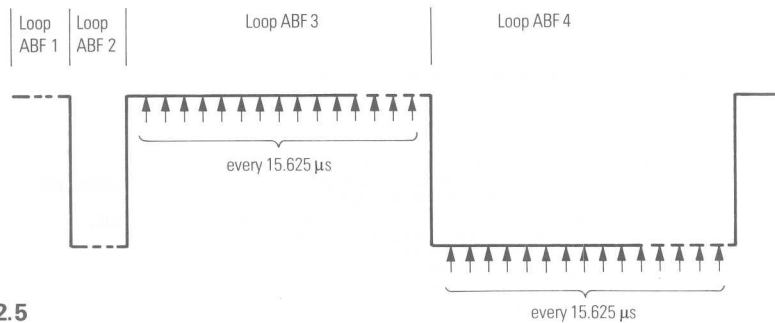


Fig. 9.2.5

addressed by content of register pair H L. Then register pair H, L is incremented and the content of register C is transferred to this memory byte. The register pair H, L is again incremented to avoid that the last memory byte is overwritten by the reset result. Now it is checked how many measurements have been taken. The total number of measurements is in register D. If the number is less than 16, a return to symbolic address ABF0 is realized and then another pulse length as well as pulse interval are measured and loaded to the next following memory bytes. This event is repeated 16 times as long as a return to main program is forced.

The measurement is faultless as long as a minimum of one strobe per pulse length and one per pulse period is realized. The other limit is set by the storage maximum with 8 bit. It is 255 or 0FFH. If a pulse period is longer than 255 strobes, register B starts again to count at 0 and an erroneous value will be achieved later when the average is taken. To avoid this false measurement the subroutine "Test für Impulswiederholungsfrequenz" (pulse repetition frequency) is called before the subroutine "Tastverhältnis" (duty cycle) runs. This program checks as to whether pulse repetition period does not exceed 4 ms. In principle this test can also be made by subroutine "Tastverhältnis" (duty cycle), but in this case the accuracy would be decreased by a factor of 2, because the INR-instruction sets no carry-bit which can be utilized to indicate a counter overflow. Therefore instructions MVI A, 01; ADD B; JC FEHL and MOV D, A have to be used, that means 28 clock cycles are now required instead of 5 cycles of the INR-instruction. Together with the instructions which have not been changed, an increase of a factor 2 is obtained.

Subroutine "Test für Impulswiederholungsfrequenz" (test for pulse repetition frequency)

This subroutine releases an error message when the pulse repetition period is longer than 4 ms, because this results in an overflow of register B, when the program "Tastverhältnis" (duty cycle) is running. The loops test 1 and test 2 correspond to loops ABF0 and ABF1 (see listing of fig. 9.2.3). At loops test 3 and test 4 only the content of register B is always incremented. An overflow immediately results in releasing an error message. When no overflow occurs after loops test 3 and test 4 have been passed the content of register B is compared with the hexadecimal number 9BH which corresponds to the register B content

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('MITTELWERTBILDUNG')
		2	;FUNKTION:DIE 16 UEBERGEHENEN MESSWERTE WERDEN JEDER FUER
		3	;SICH AUFADDIERT UND DURCH 16 GETEILT.
		4	;UEBERGABE DER MESSWERTE: SPEICHERSTELLE,+2,+4,+6,USW.
		5	;ERGEBNIS:SPEICHERST.+20H+22H
		6	;ANFANGADRESSE DER SPEICHERSTELLE IN REG. H,L.
		7	EXTRN DIVID
		8	PUBLIC MITW
		9	CSEG
0000	AF	10	MITW: XRA A ;
0001	47	11	MOV B,A ;
0002	4F	12	MOV C,A ;
0003	57	13	MOV D,A ;
0004	7E	14	SCHL1: MOV A,H ;
0005	83	15	ADD E ;
0006	5F	16	MOV E,A ;
0007	3E00	17	MVI A,0 ;
0009	17	18	RAL ;
000A	82	19	ADD D ;
000B	57	20	MOV D,A ;
000C	23	21	INX H ;
000D	23	22	INX H ;
000E	04	23	INR B ;
000F	78	24	MOV A,B ;
0010	FE10	25	CPI 10H ;
0012	C20400	26	JNZ SCHL1 ;
0015	E5	27	PUSH H ;
0016	2600	28	MVI H,00 ;
0018	2E10	29	MVI L,10H ;
001A	CD0000	30	CALL DIVID ;
001D	E1	31	POP H ;
001E	73	32	MOV H,E ;
001F	23	33	INX H ;
0020	23	34	INX H ;
0021	72	35	MOV H,D ;
0022	C9	36	RET ;
		37	END ;

PUBLIC SYMBOLS
MITW C 0000

EXTERNAL SYMBOLS
DIVID E 0000

USER SYMBOLS
DIVID E 0000 MITW C 0000 SCHL1 C 0004

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.6

of 255 in the program "Tastverhältnis" (duty cycle). When the number 255 is exceeded an error message is released, too.

Subroutine "Mittelwertbildung" (average)

The subroutine "Mittelwertbildung" (average) (see listing of **fig. 9.2.6**) adds the 16 measured values stored at the different memory bytes. The 8 bit are summed in register E. A possible overflow is stored in register D and also summed. Then the sum is divided by 16 by calling subroutine "division". The result is stored in register pair D, E.

Subroutine "Multiplikation mit 100" (multiplication with 100)

The number of pulses is multiplied by 100 to get the ratio of pulse length and pulse repetition period per cent. The listing of this subroutine is shown in **fig. 9.2.7**.

Subroutine "division"

The listing for this subroutine is shown in **fig. 9.2.8**.

Subroutine "Hexadezimal-Dezimal-Umwandlung" (Hexadecimal-to-decimal conversion)

The program, the listing of which is shown in **fig. 9.2.9**, converts a hexadecimal number in a 3-digit BCD-one.

Linking of programs

The subroutines are linked to the main program as shown in list of **fig. 9.2.10**.

Address assignment

For Mikroset 8080 application the total linked program is fixed by the locator to start address 0600H as demonstrated in **fig. 9.2.11**. The resulting code list including the correct addresses is shown in **fig. 9.2.12**.

```
ASH80 MUL100.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE PAGE 1
MULTIPLIKATION MIT 100

LOC  OBJ      SEQ      SOURCE STATEMENT
1 $TITLE('MULTIPLIKATION MIT 100')
2 ;FUNKTION:DER IM REGISTER D,E UEBERGELENE WERT WIRD MIT 100
3 ;(DEZIMAL) MULTIPLIZIERT.DAS PRODUKT WIRD IM AKKU UND DEM
4 ;REGISTERPAAR H,L AUSGEGEBEN.
5 PUBLIC MUL100
6 CSEG
0000 3E64      7 MUL100: MVI    A,64H    ;
0002 0E08      8          MVI    C,8      ;
0004 210000    9          LXI    H,0      ;
0007 29        10 MULTI1: DAD     H      ;
0008 17        11          RAL      ;
0009 D20F00    C 12          JNC     MULTI2 ;
000C 19        13          DAD     D      ;
000D CE00      14          ACI     0      ;
000F 0D        15 MULTI2: DCR     C      ;
0010 C20700    C 16          JNZ     MULTI1 ;
0013 C9        17          RET      ;
          18          END      ;

PUBLIC SYMBOLS
MUL100 C 0000

EXTERNAL SYMBOLS

USER SYMBOLS
MUL100 C 0000    MULTI1 C 0007    MULTI2 C 000F

ASSEMBLY COMPLETE, NO ERRORS
```

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.7

LOC	OBJ	SEQ	SOURCE STATEMENT
-----	-----	-----	------------------

		1	*TITLE ('DIVISION')
		2	;FUNKTION:DER DIVIDEND WIRD IM REGISTERPAAR D,E,DER DIVISOR
		3	;IM REGISTERPAAR H,L UEBERGEHEN.DER QUOTIENT STEHT IM REGI-
		4	;STERPAAR D,E,DER REST IM REGISTERPAAR H,L ALS ZWISCHEN-
		5	;SPEICHER WIRD DIE SPEICHERSTELLE 'ZELLE' BENOETIGT.
		6	
		7	EXTRN ZELLE
		8	PUBLIC DIVID
		9	CSEG
0000	220000	E 10	DIVID: SHLD ZELLE
0003	010000	11	LXI B,0
0006	C5	12	PUSH B
0007	210200	E 13	LXI H,ZELLE+2
000A	3611	14	MVI M,17
000C	7B	15	DIVID1: MOV A,E
000D	17	16	RAL
000E	5F	17	MOV E,A
000F	7A	18	MOV A,D
0010	17	19	RAL
0011	57	20	MOV D,A
0012	210200	E 21	LXI H,ZELLE+2
0015	35	22	DCR M
0016	E1	23	POP H
0017	CA3100	C 24	JZ DIVID2
001A	3E00	25	MVI A,0
001C	17	26	RAL
001D	29	27	DAD H
001E	44	28	MOV B,H
001F	85	29	ADD L
0020	2A0000	E 30	LHLD ZELLE
0023	95	31	SUB L
0024	4F	32	MOV C,A
0025	78	33	MOV A,B
0026	9C	34	SBB H
0027	47	35	MOV D,A
0028	C5	36	PUSH B
0029	D20C00	C 37	JNC DIVID1
002C	09	38	DAD B
002D	E3	39	XTHL
002E	C30C00	C 40	JMP DIVID1
0031	7A	41	DIVID2: MOV A,D
0032	2F	42	CMA
0033	57	43	MOV D,A
0034	7B	44	MOV A,E
0035	2F	45	CMA
0036	5F	46	MOV E,A
0037	C9	47	RET
		48	END

PUBLIC SYMBOLS
DIVID C 0000

EXTERNAL SYMBOLS

ZELLE E 0000

USER SYMBOLS

DIVID C 0000 DIVID1 C 000C DIVID2 C 0031 ZELLE E 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.8

ASH00 HEXBCD.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0 MODULE PAGE 1
HEXADEZIMAL-DEZIMAL-UMWANDLUNG

LOC	OBJ	SEQ	SOURCE	STATEMENT
		1	*TITLE	(HEXADEZIMAL-DEZIMAL-UMWANDLUNG)
		2	;FUNKTION: DIE IN AKKU UEBERGELENE HEXADEZIMALZAHLE WIRD IN	
		3	;EINE 3-STELLIGE BCD-ZAHLE UMGEWANDELE, UEBERGABELE IN DER MIT	
		4	;DEM REGISTERPAAR H, L ADRESSIERTEN SPEICHERSTELLE UND	
		5	;DEN DARAUFFOLGENDEN 2 SPEICHERSTELLEN.	
		6		
		7	PUBLIC	HEXBCD
		8	CSEG	
		9		
0000	23	10	HEXBCD:	INX H
0001	23	11		INX H
0002	0E64	12		MVI C, 100D
0004	CD0E00	13	CALL	HEBCD1
0007	0E0A	14		MVI C, 10D
0009	CD0E00	15	CALL	HEBCD1
000C	77	16	MOV	M, A
000D	C9	17	RET	
000E	3600	18	HEBCD1:	MVI M, 0
0010	91	19	HEBCD2:	SUB C
0011	DA1800	20		JC HEBCD3
0014	34	21		INR M
0015	C31000	22	JMP	HEBCD2
0018	81	23	HEBCD3:	ADD C
0019	2B	24		DCX H
001A	C9	25	RET	
		26	END	

PUBLIC SYMBOLS
HEXBCD C 0000

EXTERNAL SYMBOLS

USER SYMBOLS
HEBCD1 C 000E HEBCD2 C 0010 HEBCD3 C 0018 HEXBCD C 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.2.9

ISIS-II LINKER V2.1 WAS INVOKED BY:
LINK SENSOR.OBJ, TEST.OBJ, TASTV.OBJ, MITW.OBJ, MUL100.OBJ, DIVID.OBJ, HEXBCD.OBJ TO SENSOR.LNK MAP PRINT(:TO:)

LINK MAP FOR SENSOR.LNK(SENSOR)

SEGMENT INFORMATION:
START STOP LENGTH REL NAME

13DH B CODE

INPUT MODULES INCLUDED:

SENSOR.OBJ(MODULE)
TEST.OBJ(MODULE)
TASTV.OBJ(MODULE)
MITW.OBJ(MODULE)
MUL100.OBJ(MODULE)
DIVID.OBJ(MODULE)
HEXBCD.OBJ(MODULE)

Fig. 9.2.10

An insignificant reduction of the program can be realized in that numerator and dominator are not treated as 16-bit words by the division subroutine but by limiting the dominator to 8 bit. This reduction is not utilized in this application example as the subroutine "division" may universally be used by other programs for different purposes.

If the pulse repetition period is constant and if the repetition frequency is not less than 250 Hz, the subroutine "Test für Impulswiederholfrequenz" (test for pulse repetition frequency) and the output routine "FEHL" (error) at the end of the main program can be given up.

```
ISIS-II LOCATER V2.1 INVOKED BY:
-LOCATE SENSOR.LNK TO SENSOR.V1 CODE(0600H) START(0600H) MAP PRINT(:TO:) PUBLICS SYMBOLS

SYMBOL TABLE OF MODULE SENSOR
READ FROM FILE :F0:SENSOR.LNK
WRITTEN TO FILE :F0:SENSOR.V1

VALUE TYPE SYMBOL
0750H PUB SPEICH
0776H PUB ZELLE
06EAH PUB DIVID
0644H PUB FEHL
06B3H PUB MITW
06D6H PUB MUL100
064CH PUB TEST
067FH PUB TASTV
0722H PUB HEXBCD

MEMORY MAP OF MODULE SENSOR
READ FROM FILE :F0:SENSOR.LNK
WRITTEN TO FILE :F0:SENSOR.V1
MODULE START ADDRESS 0600H

START STOP LENGTH REL NAME
0600H 73CH 13DH B CODE
73DH F6BFH EF83H B MEMORY
```

Fig. 9.2.11

Codetabelle

```
0600H 3EH 8AH D3H FFH CDH 4CH 06H CDH 7FH 06H 21H 50H 07H CDH B3H 06H
0610H 21H 51H 07H CDH B3H 06H CDH D6H 06H 54H 5DH 21H 70H 07H 6EH 26H
0620H 00H AFH 32H 76H 07H CDH EAH 06H 21H 76H 07H CDH 22H 07H 21H 76H
0630H 07H 5EH 23H AFH 7EH 17H 17H 17H 17H B3H 5FH 23H 56H EBH CDH C0H
0640H 01H C3H 00H 06H 26H FFH 2EH FFH CDH C0H 01H C9H 06H 00H DBH FEH
0650H E6H 00H C2H 4EH 06H DBH FEH E6H 00H CAH 55H 06H 3EH 01H 80H DAH
0660H 44H 06H 47H DBH FEH E6H 00H C2H 5CH 06H 3EH 01H 80H DAH 44H 06H
0670H 47H DBH FEH E6H 00H CAH 6AH 06H 78H D6H 9BH D2H 44H 06H C9H 21H
0680H 50H 07H 16H 00H 06H 00H 0EH 00H DBH FEH E6H 00H C2H 88H 06H DBH
0690H FEH E6H 00H CAH 8FH 06H 14H DBH FEH 04H E6H 00H C2H 97H 06H 48H
06A0H DBH FEH 04H E6H 00H CAH A0H 06H 70H 23H 71H 23H 7AH FEH 10H C2H
06B0H 84H 06H C9H AFH 47H 4FH 57H 7EH 83H 5FH 3EH 00H 17H 82H 57H 23H
06C0H 23H 04H 78H FEH 10H C2H B7H 06H 5EH 26H 00H 2EH 10H CDH EAH 06H
06D0H E1H 73H 23H 23H 72H C9H 3EH 64H 0EH 00H 21H 00H 00H 29H 17H D2H
06E0H E5H 06H 19H CEH 00H 0DH C2H DDH 06H C9H 22H 76H 07H 01H 00H 00H
06F0H C5H 21H 78H 07H 36H 11H 7BH 17H 5FH 7AH 17H 57H 21H 78H 07H 35H
0700H E1H CAH 1BH 07H 3EH 00H 17H 29H 44H 85H 2AH 76H 07H 95H 4FH 78H
0710H 9CH 47H C5H D2H F6H 06H 09H E3H C3H F6H 06H 7AH 2FH 57H 7BH 2FH
0720H 5FH C9H 23H 23H 0EH 64H CDH 30H 07H 0EH 0AH CDH 30H 07H 77H C9H
0730H 36H 00H 91H DAH 3AH 07H 34H C3H 32H 07H 81H 2BH C9H
*
```

Fig. 9.2.12

9.3 Program for Measuring a Period

Conventional frequency counters operate in accordance to the principle of counting zero-crossings per second. This method, however, is disadvantageous for low frequencies, because a long measuring interval is required for determining the frequency with an acceptable accuracy. If, e.g., a frequency of 10 Hz is to be measured with an accuracy of 1%, a measuring time of 10 s is required. Therefore conventional frequency counters do not directly count low frequencies but they measure the period. In the following a method is described for measuring frequencies between 1 Hz and 30 kHz. The accuracy, however, decreases with increasing frequency. The result is already available after two measured periods.

If the signal, the frequency of which is to be measured, is already a square wave with TTL-levels, it can be directly applied to input PC₇. If the signal is a sine wave, then a square wave has to be generated by using additional Schmitt-trigger-ICs.

The program listing is shown in **fig. 9.3.1**. First the I/O-peripheral interface IC SAB 8255 is programmed in that PC₇ operates as input. Register pair H, L functions

```

ASM80 PDHSG.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE PAGE 1
PERIODENDAUERMESSUNG

LOC OBJ      SEQ      SOURCE STATEMENT

1 $TITLE('PERIODENDAUERMESSUNG')
2 ;FUNKTION:AN KLEMMEN PC7 WIRD GEPRUEFT, WIE LANGE JEWEILS
3 ;H- ODER L-SIGNAL ANLIEGT. DIE LAENGE DES SIGNALS IST
4 ;PROPORTIONAL DER ANZAHL DURCHLAUFENER SCHLEIFEN, DIE
5 ;IN REGISTERPAAR H, L EINGEZAHLT WERDEN.
6 PORTC EQU 0FEH
7 ORG 0600H ;
8 MVI A, 80H ;
9 OUT 0FFH ;
10 ABF0: MVI H, 0 ;
11 MVI L, 0 ;
12 ABF1: IN PORTC ;
13 ANI 80H ;
14 JNZ ABF1 ;
15 ABF2: IN PORTC ;
16 ANI 80H ;
17 JZ ABF2 ;
18 ABF3: IN PORTC ;
19 INX H ;
20 ANI 80H ;
21 JNZ ABF3 ;
22 ABF4: IN PORTC ;
23 INX H ;
24 ANI 80H ;
25 JZ ABF4 ;
26 CALL 01C0H ; AUSGABE AUF ADRESSANZEIGE
27 JMP ABF0 ;
28 END

PUBLIC SYMBOLS
EXTERNAL SYMBOLS
USER SYMBOLS
ABF0 A 0604 ABF1 A 0608 ABF2 A 060F ABF3 A 0616 ABF4 A 061E PORTC A 00FE

ASSEMBLY COMPLETE, NO ERRORS

```

Note: For translation of the German comments pls. see preceding text.

Fig. 9.3.1

as loop counter. It is set to zero at the symbolic address ABF0. Two scanning loops ABFR1 and ABFR2 are provided for forcing a defined start for counting pulse length (H-duration) and pulse repetition period (L-interval). Loop ABFR1 is not left as long as a signal with H-level is applied to PC₇. When the signal changes from H to L-level, then the program continues to loop ABFR2 and remains as long as an H-level is applied to input PC₇ as shown in **fig. 9.3.2**. Every 15.625 µs the signal level at input PC₇ is scanned by loop ABFR3 and the content of register pair H, L is incremented. When the signal changes from H to L-level loop ABFR3 is left and the number of scans within loop ABFR4 is added to the content of register pair H, L.

Loop ABFR4 is left when the signal at PC₇ changes from L to H-level. The result, i.e. the content of register pair H, L is indicated on the address display of the Mikroset 8080.

For frequencies greater than 250 Hz the last significant byte of the result is only required. The hexadecimal number is to be multiplied by 15.625 µs and thus the period is determined.

If a direct frequency indication is required the decimal number 64000 $\hat{=}$ hexadecimal 0FA00 has to be divided by the content of register pair H, L. Then the result is indicated on the address display as frequency in Hz.

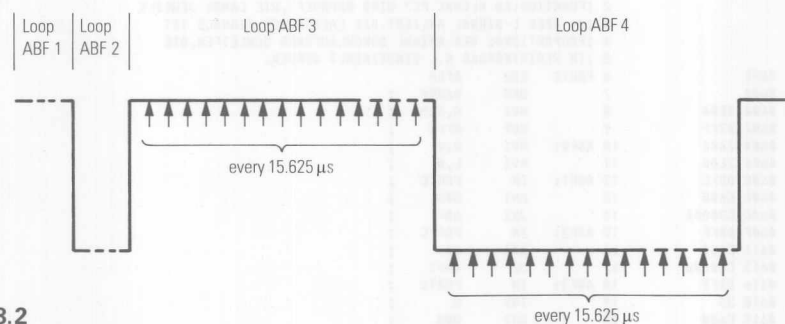


Fig. 9.3.2

Components for circuit 9.3.1

			Ordering code
1 Keyboard encoder with intermediate memory	S600 E5-T		Q67100-Z133-V5
1 8-bit I/O-interface IC	SAB 8212-P		Q67020-P3
10 Diodes	BAW 76		Q62702-A397
1 Polypropylene-capacitor	100 pF/630 V		B33063-B6101-H

9.4 Program for Searching and Printing of Memory Word Addresses with Special Content

The program described in the following is applicable for all 8080/8085-systems. The structogram is shown in **fig. 9.4.1**. This program prints all addresses of memory words, the content of which is equal to a set code. It operates user-oriented, i.e. the user is requested by text on the CRT to make the desired inputs like code word, start and end addresses. These three inputs are serially required. If

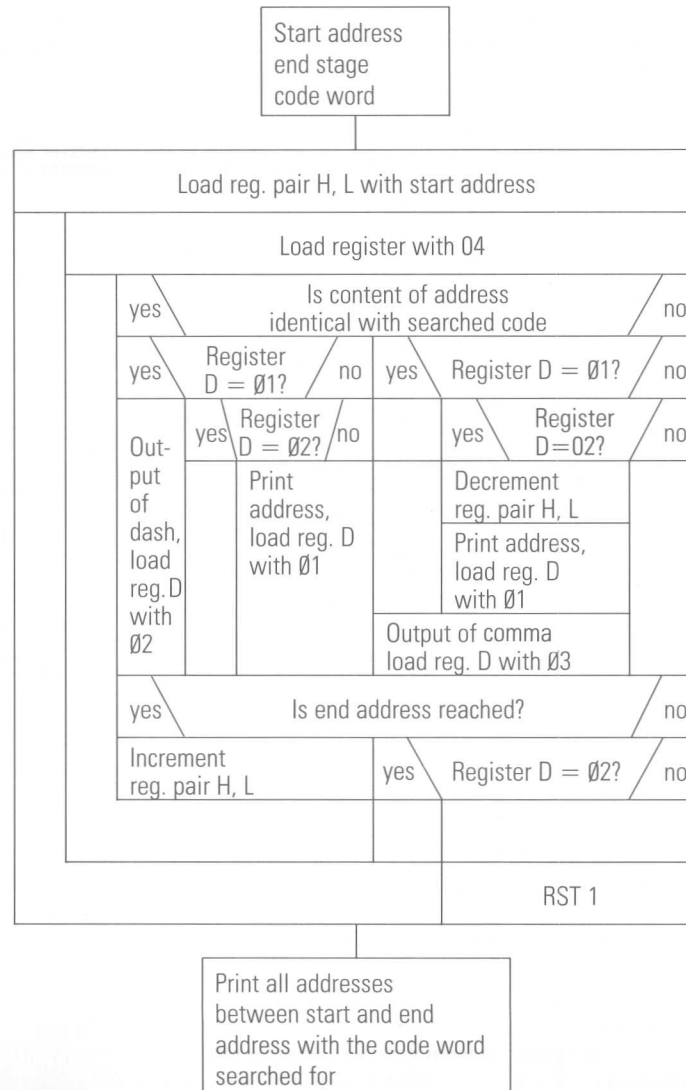


Fig. 9.4.1

the user makes an input mistake, the error message "fehlerhafte Eingabe" (input fault) and again the last requirement are displayed. Addresses and code word have to be input in hexadecimal code and the input is finished by "CR".

The total program consists of a main part and of subroutines, which are available as modules with relative addresses. After the assembling all modules are linked and located, i.e. the absolute addresses of the memory bytes are determined by the locator. **Fig. 9.4.2** shows the main program listing. The start addresses of subroutines and texts are indicated as externals.

ASM80 SUCODE.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0
SUCHEN EINES CODES

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE ('SUCHEN EINES CODES')
		2	;DAS PROGRAMM DRUCKT DIE ADRESSEN DER SPEICHERSTELLEN AUS,
		3	;DEREN INHALT MIT DEM EINGEGEBENEN CODE UEBEREINSTIMMT.
		4	EXTRN ANENCO
		5	EXTRN ANFA
		6	EXTRN AUSG3
		7	EXTRN CO
		8	EXTRN ENDA
		9	EXTRN NMOUT
		10	EXTRN PRCODE
		11	EXTRN TEXT11
		12	EXTRN TEXT12
		13	EXTRN TEXTX
		14	CSEG
0000	310000	S 15	START: LXI SP,STACK;
0003	210000	E 16	LXI H,TEXT11;
0006	CD0000	E 17	CALL AUSG3 ;
0009	210000	E 18	LXI H,TEXT12;
000C	220000	E 19	SHLD TEXTX ;
000F	CD0000	E 20	CALL ANENCO
0012	3A0000	E 21	LDA PRCODE
0015	5F	22	MOV E,A ;
0016	2A0000	E 23	LHLD ANFA
0019	1604	24	MVI D,04H ;
001B	CD4900	C 25	SCHL1: CALL AUSGA ;
001E	3A0000	E 26	SCHL2: LDA ENDA ;
0021	8D	27	CMP L ;
0022	C23000	C 28	JNZ FORTS ;
0025	3A0100	E 29	LDA ENDA+1 ;
0028	8C	30	CMP H ;
0029	C23000	C 31	JNZ FORTS ;
002C	CD4900	C 32	CALL AUSGA ;
002F	CF	33	RST 1 ;
0030	23	34	FORTS: INX H ;
0031	7E	35	MOV A,M ;
0032	8B	36	CMP E ;
0033	CA6600	C 37	JZ STRICH ;
0036	3E01	38	MVI A,01H ;
0038	8A	39	CMP D ;
0039	CASB00	C 40	JZ KOMMA ;
003C	3E03	41	MVI A,03H ;
003E	8A	42	CMP D ;
003F	CA1E00	C 43	JZ SCHL2 ;
0042	2B	44	DCX H ;
0043	CD4900	C 45	CALL AUSGA ;
0046	C35B00	C 46	JMP KOMMA ;
0049	3E01	47	AUSGA: MVI A,01H ;
004B	8A	48	CMP D ;
004C	C8	49	RZ ;
004D	7E	50	MOV A,M ;
004E	8B	51	CMP E ;
004F	C0	52	RNZ ;

Note: For translation of the German comments pls. see preceding text.

Fig. 9.4.2 (Page 1)

LOC	OBJ	SEQ	SOURCE	STATEMENT
0050	7C	53	MOV	A,H ;
0051	CD0000	E 54	CALL	NROUT ;
0054	7D	55	MOV	A,L ;
0055	CD0000	E 56	CALL	NROUT ;
0058	1601	57	MVI	D,01H ;
005A	C9	58	RET	;
005B	0E2C	59 KOMMA:	MVI	C,2CH ;
005D	CD0000	E 60	CALL	C0 ;
0060	1603	61	MVI	D,03H ;
0062	23	62	INX	H ;
0063	C31B00	C 63	JMP	SCHL1 ;
0066	3E02	64 STRICH:	MVI	A,02H ;
0068	BA	65	CMP	D ;
0069	CA1E00	C 66	JZ	SCHL2 ;
006C	3E01	67	MVI	A,01H ;
006E	BA	68	CMP	D ;
006F	C21B00	C 69	JNZ	SCHL1 ;
0072	0E2D	70	MVI	C,2DH ;
0074	CD0000	E 71	CALL	C0 ;
0077	1602	72	MVI	D,02H ;
0079	C31E00	C 73	JMP	SCHL2 ;
0080		C 74	END	START

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

ANENCO E 0000 ANFA E 0000 AUSG3 E 0000 C0 E 0000 ENDA E 0000 NROUT E 0000 PRCODE E 0000
 TEXT11 E 0000 TEXT12 E 0000 TEXTX E 0000

USER SYMBOLS

ANENCO E 0000 ANFA E 0000 AUSG3 E 0000 AUSGA C 0049 C0 E 0000 ENDA E 0000 FORTS C 0030
 KOMMA C 005B NROUT E 0000 PRCODE E 0000 SCHL1 C 001B SCHL2 C 001E START C 0000 STRICH C 0066
 TEXT11 E 0000 TEXT12 E 0000 TEXTX E 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.4.2 (Page 2)

The start address for the text is intermediately stored into the memory word text X to be flexible for text output of the code word. In this case text 12 is used as text X. The input of start and end addresses as well as the code word is realized by subroutine ANENCO (see fig. 9.4.3 and fig. 9.4.4). First step of this subroutine is to push the stack pointer to memory bytes STRCKA and STRCKA+1. This measure is necessary as subroutines can be interrupted without continuing at the last address when an error message occurs.

Then memory bytes RCKAD and RCKAD+1 are loaded with return address R1 and the output of text 4 "Anfangsadresse?" (start address) is released. Now the console expects the input of start address. Each character is checked for plausibility and 'CR' finishes the procedure. The starting address is stored in memory byte ANFA and ANFA+1.

Now memory bytes RCKAD and RCKAD+1 are loaded with return address R2 and text 5 "Endadresse" (end address) is displayed. The end address has now to be indicated on the console. It is stored in memory bytes ENDA and ENDA+1.

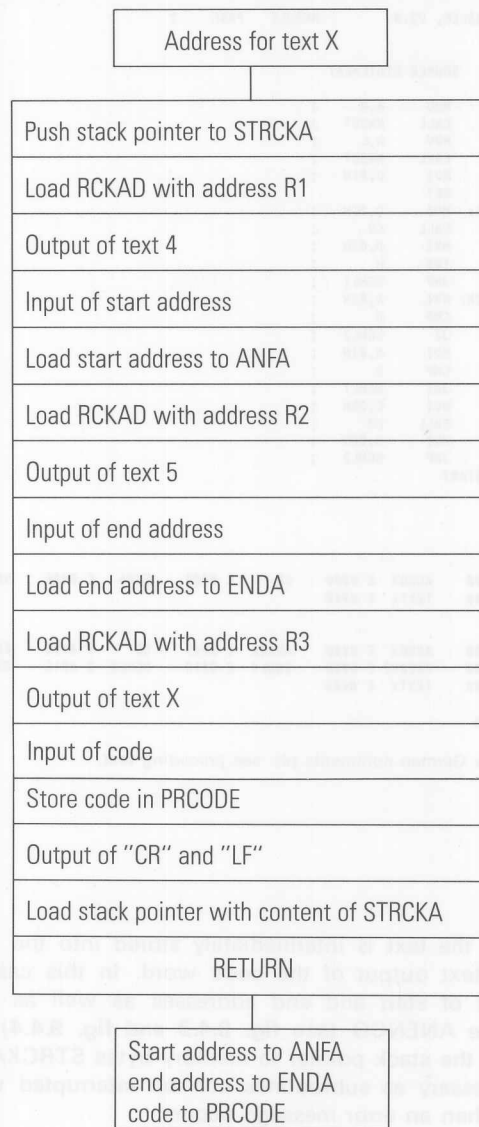


Fig. 9.4.3

The texts are listed in the text module shown in **fig. 9.4.5**.

After loading memory words RCKAD and RCKAD+1 with return address R3 the text X, in this case text 12 "gesuchtes Codewort?" (code word searched for), is displayed. The code word, being typed in, is loaded in memory word PCODE.

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('EINGABE VON ANFANGSADRESSE,ENDADRESSE UND CODE')
		2	EXTRN ANFA
		3	EXTRN AUSG3
		4	EXTRN CO
		5	EXTRN ENDA
		6	EXTRN PCODE
		7	EXTRN RCKAD
		8	EXTRN EING1
		9	EXTRN TEXT4
		10	EXTRN TEXT5
		11	EXTRN TEXTX
		12	PUBLIC ANENCO
		13	CSEG
0000	210600	C 14	ANENCO: LXI H,R1 ;
0003	220000	E 15	SHLD RCKAD ;
0006	210000	E 16	R1: LXI H,TEXT4 ;
0009	CD0000	E 17	CALL AUSG3 ;
000C	210000	E 18	LXI H,ANFA ;
000F	1E05	19	MVI E,5 ;
0011	CD0000	E 20	CALL EING1 ;
0014	211400	C 21	R2: LXI H,R2 ;
0017	220000	E 22	SHLD RCKAD ;
001A	210000	E 23	LXI H,TEXT5 ;
001D	CD0000	E 24	CALL AUSG3 ;
0020	210000	E 25	LXI H,ENDA ;
0023	1E05	26	MVI E,5 ;
0025	CD0000	E 27	CALL EING1 ;
0028	212800	C 28	R3: LXI H,R3 ;
002B	220000	E 29	SHLD RCKAD ;
002E	2A0000	E 30	LHLD TEXTX ;
0031	CD0000	E 31	CALL AUSG3 ;
0034	21FFFF	E 32	LXI H,PCODE-1 ;
0037	1E03	33	MVI E,3 ;
0039	CD0000	E 34	CALL EING1 ;
003C	0E0D	35	MVI C,0DH ;
003E	CD0000	E 36	CALL CO ;
0041	0E0A	37	MVI C,0AH ;
0043	CD0000	E 38	CALL CO ;
0046	C9	39	RET ;
		40	END

PUBLIC SYMBOLS
ANENCO C 0000

EXTERNAL SYMBOLS
ANFA E 0000 AUSG3 E 0000 CO E 0000 EING1 E 0000 ENDA E 0000 PCODE E 0000 RCKAD E 0000
TEXT4 E 0000 TEXT5 E 0000 TEXTX E 0000

USER SYMBOLS
ANENCO C 0000 ANFA E 0000 AUSG3 E 0000 CO E 0000 EING1 E 0000 ENDA E 0000 PCODE E 0000
R1 C 0006 R2 C 0014 R3 C 0028 RCKAD E 0000 TEXT4 E 0000 TEXT5 E 0000 TEXTX E 0000

ASSEMBLY COMPLETE, NO ERRORS

Fig. 9.4.4

Output of characters CR and LF assures that all displayed addresses start with a new line on the CRT. Now the stack pointer is loaded with the address being pushed to STRCKA and STRCKA+1.

Program ANENCO uses subroutine "AUSG3" as well as "EING1". Both are described later.

The main program runs as follows. Register pair H, L is loaded with the start address and register D is loaded with the content 04. Then it is checked as to whether the content of the memory word for start address is identical with the code word searched for. If this is the case at the first comparison, the second question whether the content of register D is 01 can only be answered with "no". Also the next question, whether register D contains 02 can be answered with "no". The first valid address is now printed by using subroutine NMOUT (see section 9.7).

ASM80 TEXTE.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0
TEXTE

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	\$TITLE('TEXTE')
		2	PUBLIC TEXT4
		3	PUBLIC TEXT5
		4	PUBLIC TEXT7
		5	PUBLIC TEXT11
		6	PUBLIC TEXT12
		7	CSEG
0000	0D	8	TEXT4: DB 0DH,0AH,'ANFANGSADRESSE DES SPEICHERBEREICHES ?',03H
0001	0A		
0002	414E4641		
0006	4E475341		
000A	44524553		
000E	53452044		
0012	45532053		
0016	50454943		
001A	48455242		
001E	45524549		
0022	43484553		
0026	203F		
0028	03		
0029	0D	9	TEXT5: DB 0DH,0AH,'ENDADRESSE DES SPEICHERBEREICHES ?',03H
002A	0A		
002B	454E4441		
002F	44524553		
0033	53452044		
0037	45532053		
003B	50454943		
003F	48455242		
0043	45524549		
0047	43484553		
004B	203F		
004D	03		
004E	0D	10	TEXT7: DB 0DH,0AH,'FEHLERHAFTE EINGABE',0DH,0AH,03H
004F	0A		
0050	4645484C		
0054	45524841		
0058	46544520		
005C	45494E47		
0060	414245		
0063	0D		
0064	0A		
0065	03		
0066	50454C4B	11	TEXT11: DB 'PELKA SUCH-CODE-PROGRAMM',0DH,0AH,03H
006A	41205355		
006E	43482043		
0072	4F44452D		
0076	50524F47		
007A	52414D4D		
007E	0D		
007F	0A		
0080	03		
0081	0D	12	TEXT12: DB 0DH,0AH,'GESUCHTES CODEWORT ?',03H

Note: For translation of the German comments pls. see preceding text.

Fig. 9.4.5 (Page 1)


```

ISIS-II 0000/0005 MACRO ASSEMBLER, V2.0      MODULE PAGE 2
TEXT0
LOC OBJ      SEQ      SOURCE STATEMENT
0082 0A
0083 47455355
0087 43485445
0088 5320434F
008F 4445574F
0093 5254203F
0097 03
13 END

PUBLIC SYMBOLS
TEXT11 C 0066 TEXT12 C 0081 TEXT4 C 0000 TEXT5 C 0029 TEXT7 C 004E

EXTERNAL SYMBOLS

USER SYMBOLS
TEXT11 C 0066 TEXT12 C 0081 TEXT4 C 0000 TEXT5 C 0029 TEXT7 C 004E

ASSEMBLY COMPLETE, NO ERRORS

```

Fig. 9.4.5 (Page 2)

Register D is loaded with 01 as criterion for the fact that an address had been printed. Now the end address check is processed. Assuming the end address is not yet reached, then register pair H, L is incremented to check the content of the next memory word. It is now assumed that this memory byte contains the code word searched for. Content of register D is 01 due to the output of the previous address. The console prints a dash and loads register D with 02. If the end address has not yet been reached register pair H, L is again incremented to check the content of the next memory word. It is again assumed that the content of this memory byte is identical with the searched code. But it is already the end address. Register D is still loaded with 02 by the previous dash. The question for end address is answered with "yes". Then it is again questioned whether register D is loaded with 02 because the last address has to be printed. By branching the program it returns to its start and loads register D with 04. A second check is made whether the content of the memory word address is identical with the code word. The answer is "yes". However, content of register D is neither 01 nor 02. The address is printed and register D is loaded with 01 for demonstration of a printing. The second question for end address is "yes". Register D has not the content of 02. The branching leads to instruction RST1, which causes a program jump to memory word 0008, where a jump-instruction is stored. Now the program jumps either into a monitor program or into the SME 800-operating-system.

Now the cases, where the content of the memory words are not identical with the code word searched for, have to be described. There are six different cases.

- 1st No address with a content being identical with the code word searched for has been found.

- 2nd Code word and content of the previous address are identical. An address had been printed.
- 3rd Code word and content of the previous address are identical and a dash had been printed.
- 4th Code word and content of the previous address are not identical. A comma had been printed.
- 5th Code word and content of the previous address are identical, but nothing had been output, because a dash had previously been printed.
- 6th Code word and content of the previous address are not identical; nothing had been output, as a comma had previously been printed.

Case 1:

The content of register D is 04. The questions as to whether its content is 01 or 02 are answered with "no". The end address is also not reached. Therefore only register pair H, L is incremented as long as the content of an address is identical with the code word searched for.

Case 2:

The content of register D is 01. A comma is printed and register D is loaded with 03 for comma identification. If the end address is not yet reached, a loop leads to another question as to whether the code word is identical with the content of the memory word address or not.

Case 3:

This case is a complicated one, because a dash had been printed under the assumption that more memory word addresses, the content of which is identical with the code word, will follow. However, in this case the last address with identical content has still to be printed. Register D has the content 02. Then register pair H,L is decremented, the address is printed and register D is loaded with 01. Thereafter a comma is printed and the register is loaded with 03. Now the address is reached for the second time by incrementing register pair H,L. However, case 4 occurs now.

Case 4:

Register D is loaded with 03. As the content of the memory word address is not identical with the code word nothing happens. It is only questioned whether end address is reached or not. Register pair H,L is incremented again and the program returns at its start.

Case 5:

This one corresponds to case no. 3, since register D is still loaded with 03 from the last printing of the dash.

Case 6:

This corresponds to the case no. 4, because a comma and thereafter no other characters had been printed at one of the previous addresses, the content of which is identical with the code word.

The case that one or more addresses, the content of which is identical with the code word, follow after a dash had been printed, is not yet described. In this case register D is loaded with 02. The program runs in a loop asking as to whether the end address is reached, incrementing register pair H,L and scanning whether the content of the new memory word address is identical with the code word or not.

As already mentioned the main program includes the module SUCODE.SRC and 9 subroutines, being written also as modules, and two text-modules. To be able to run the program on different systems like SME 800, SMP, etc. another module ADZUW1 is added. It determines the memory word address ANFA, ENDA, PRCODE, RCKA, STRCKA and text X (see **fig. 9.4.6**). If a system design kit SIKIT-DK/8080 (no longer in the Siemens delivery program) is used, the start addresses of the subroutines, existing already in the SIKIT-monitor (see **fig. 9.4.7**), can be found

```
ASH00 ADZUW1.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE PAGE 1
ADRESSZUWEISUNG

LOC OBJ      SEQ      SOURCE STATEMENT

                1 $TITLE('ADRESSZUWEISUNG')
                2 PUBLIC ANFA
                3 PUBLIC ENDA
                4 PUBLIC PRCODE
                5 PUBLIC RCKAD
                6 PUBLIC STRCKA
                7 PUBLIC TEXTX
F2F0            8 ANFA    EQU 0F2F0H
F2F2            9 ENDA    EQU 0F2F2H
F2F8           10 PRCODE  EQU 0F2F8H
F2FA           11 RCKAD   EQU 0F2FAH
F2FE           12 STRCKA  EQU 0F2FEH
F2FC           13 TEXTX   EQU 0F2FCH
                14 END

PUBLIC SYMBOLS
ANFA  A F2F0  ENDA  A F2F2  PRCODE A F2F8  RCKAD  A F2FA  STRCKA A F2FE  TEXTX  A F2FC

EXTERNAL SYMBOLS

USER SYMBOLS
ANFA  A F2F0  ENDA  A F2F2  PRCODE A F2F8  RCKAD  A F2FA  STRCKA A F2FE  TEXTX  A F2FC

ASSEMBLY COMPLETE, NO ERRORS
```

Note: For translation of the German comments pls. see preceding text.

Fig. 9.4.6

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE('ADRESSZUWEISUNG')
		2	PUBLIC ANFA
		3	PUBLIC CI
		4	PUBLIC CNVBN
		5	PUBLIC CO
		6	PUBLIC DIGTB
		7	PUBLIC ECHO
		8	PUBLIC ENDA
		9	PUBLIC GETCH
		10	PUBLIC NMOUT
		11	PUBLIC PRCODE
		12	PUBLIC PRVAL
		13	PUBLIC RCKAD
		14	PUBLIC STRCKA
		15	PUBLIC TEXTX
		16	PUBLIC VALDG
10F0		17	ANFA EQU 10F0H
03FD		18	CI EQU 03FDH
01DA		19	CNVBN EQU 01DAH
03FA		20	CO EQU 03FAH
03BF		21	DIGTB EQU 03BFH
01F4		22	ECHO EQU 01F4H
10F2		23	ENDA EQU 10F2H
021B		24	GETCH EQU 021BH
02C3		25	NMOUT EQU 02C3H
10F8		26	PRCODE EQU 10F8H
02DE		27	PRVAL EQU 02DEH
10FA		28	RCKAD EQU 10FAH
10FE		29	STRCKA EQU 10FEH
10FC		30	TEXTX EQU 10FCH
036F		31	VALDG EQU 036FH
		32	END

PUBLIC SYMBOLS

ANFA	A 10F0	CI	A 03FD	CNVBN	A 01DA	CO	A 03FA	DIGTB	A 03BF	ECHO	A 01F4	ENDA	A 10F2
GETCH	A 021B	NMOUT	A 02C3	PRCODE	A 10F8	PRVAL	A 02DE	RCKAD	A 10FA	STRCKA	A 10FE	TEXTX	A 10FC
VALDG	A 036F												

EXTERNAL SYMBOLS

USER SYMBOLS

ANFA	A 10F0	CI	A 03FD	CNVBN	A 01DA	CO	A 03FA	DIGTB	A 03BF	ECHO	A 01F4	ENDA	A 10F2
GETCH	A 021B	NMOUT	A 02C3	PRCODE	A 10F8	PRVAL	A 02DE	RCKAD	A 10FA	STRCKA	A 10FE	TEXTX	A 10FC
VALDG	A 036F												

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.4.7

in the module. Besides that it contains also the start addresses for CI and CO for serial input or output.

If a SME 800 is used, the system-LIB is also linked for the start address CI and CO.

Fig. 9.4.8 shows the listing for linker and fig. 9.4.9 indicates the listing for the locator, if a SME 800 is used. For using a SIKIT the locator listing is shown in fig. 9.4.10 and fig. 9.4.11.

In the latter case less subroutines have to be linked as they exist already in the monitor program. As the addresses of these monitor programs are listed as "publics" in the address allocation module, they can also be found in the locator listing as "publics".

The subroutines are described in the following sections 9.5 to 9.7 for those not knowing them.

```

ISIS-II LINKER V2.1 WAS INVOKED BY:
LINK SUCODE.OBJ,ANENCO.OBJ,AUSG3.OBJ,EING1.OBJ,NMOUT1.OBJ,PRVAL1.OBJ,FEHLER.OBJ,&
CNVBN.OBJ,GETCH.OBJ,VALDG.OBJ,ADZUW1.OBJ,TEXTE.OBJ,SYSTEM.LIB TO SUCOD1.LNK MAP PRINT(:TO:)

LINK MAP FOR SUCOD1.LNK(SUCOD1)

SEGMENT INFORMATION:
  START  STOP LENGTH REL NAME

      20EH  B  CODE

INPUT MODULES INCLUDED:
SUCODE.OBJ(MODULE)
ANENCO.OBJ(MODULE)
AUSG3.OBJ(MODULE)
EING1.OBJ(MODULE)
NMOUT1.OBJ(MODULE)
PRVAL1.OBJ(MODULE)
FEHLER.OBJ(MODULE)
CNVBN.OBJ(MODULE)
GETCH.OBJ(MODULE)
VALDG.OBJ(MODULE)
ADZUW1.OBJ(MODULE)
TEXTE.OBJ(MODULE)
SYSTEM.LIB(CI)
SYSTEM.LIB(CO)

```

Fig. 9.4.8

```

ISIS-II LOCATER V2.1 INVOKED BY:
-LOCATE SUCOD1.LNK TO SUCODE CODE(0F000H) START(0F000H) STACK(0EFFFH) &
**ORDER(STACK,CODE,MEMORY) MAP PUBLICS SYMBOLS PRINT(:TO:)

SYMBOL TABLE OF MODULE SUCOD1
READ FROM FILE :F0:SUCOD1.LNK
WRITTEN TO FILE :F0:SUCODE

VALUE TYPE SYMBOL

F2F2H PUB ENDA
F2F0H PUB ANFA
F2FCH PUB TEXTX
F2FEH PUB STRCKA
F2FAH PUB RCKAD
F2F8H PUB PRCODE
F803H PUB CI
F809H PUB CO
F152H PUB GETCH
F159H PUB VALDG
F13CH PUB FEHLER
F124H PUB PRVAL
F07CH PUB ANENCO
F149H PUB CNVBN
F105H PUB WEITER
F109H PUB NMOUT
F19FH PUB TEXT5
F176H PUB TEXT4
F1C4H PUB TEXT7
F0C3H PUB AUSG3
F0CFH PUB EING1
F1DCH PUB TEXT11
F1F7H PUB TEXT12

MEMORY MAP OF MODULE SUCOD1
READ FROM FILE :F0:SUCOD1.LNK
WRITTEN TO FILE :F0:SUCODE
MODULE START ADDRESS F000H

START  STOP LENGTH REL NAME

F000H F20DH  20EH  B  CODE
F20EH F6BFH  4B2H  B  MEMORY

```

Fig. 9.4.9

ISIS-II LINKER V2.1 WAS INVOKED BY:
 LINK SUCODE.OBJ,ANENCO.OBJ,AUSG3.OBJ,EING1.OBJ,FEHLER.OBJ,ADZUW2.OBJ,&
 TEXTE.OBJ TO SUCOD2.LNK MAP PRINT(:TO:)

LINK MAP FOR SUCOD2.LNK(SUCOD2)

SEGMENT INFORMATION:
 START STOP LENGTH REL NAME

1AEH B CODE

INPUT MODULES INCLUDED:

SUCODE.OBJ(MODULE)
 ANENCO.OBJ(MODULE)
 AUSG3.OBJ(MODULE)
 EING1.OBJ(MODULE)
 FEHLER.OBJ(MODULE)
 ADZUW2.OBJ(MODULE)
 TEXTE.OBJ(MODULE)

Fig. 9.4.10

ISIS-II LOCATER V2.1 INVOKED BY:
 -LOCATE SUCOD2.LNK TO SUCODE.V2 CODE(4800H) START(4800H) STACK(10EFH) ORDER(STACK,CODE,MEMORY) &
 **MAP PUBLICS SYMBOLS PRINT(:TO:)

SYMBOL TABLE OF MODULE SUCOD2
 READ FROM FILE :F0:SUCOD2.LNK
 WRITTEN TO FILE :F0:SUCODE.V2

VALUE TYPE SYMBOL

021BH PUB GETCH
 036FH PUB VALDG
 10F2H PUB ENDA
 10F0H PUB ANFA
 02DEH PUB PRVAL
 10FCH PUB TEXTX
 01DAH PUB CNVBN
 10FEH PUB STRCKA
 02C3H PUB NHOUT
 10FAH PUB RCKAD
 01F4H PUB ECHO
 10F8H PUB PRCODE
 03FDH PUB CI
 03FAH PUB CO
 03BFH PUB DIGTB
 4909H PUB FEHLER
 487CH PUB ANENCO
 4905H PUB WEITER
 493FH PUB TEXTS
 4916H PUB TEXT4
 4964H PUB TEXT7
 48C3H PUB AUSG3
 48CFH PUB EING1
 497CH PUB TEXT11
 4997H PUB TEXT12

MEMORY MAP OF MODULE SUCOD2
 READ FROM FILE :F0:SUCOD2.LNK
 WRITTEN TO FILE :F0:SUCODE.V2
 MODULE START ADDRESS 4800H

START STOP LENGTH REL NAME

4800H 49ADH 1AEH B CODE
 49AEH F6BFH AD12H B MEMORY

Fig. 9.4.11

9.5 Output Program for Texts of Any Length

The program described in the following is originally a subroutine. Register pair H,L is loaded with the start address of the text, i.e. before the subroutine is called. Character "ETX" (03H) is the criterion for end of text. The structogram is shown in **fig. 9.5.1** and **fig. 9.5.2** indicates the listing. The content of the memory word, the actual address of which is in register pair H,L, is transferred to register C. Then it is checked as to whether the content of the actual memory is 03H. If not the character output is realized by calling subroutine CO. Then register pair H,L, i.e. the address, is incremented. A loop returns to program start.

If the end character 03H is in the memory word with the actual address a return to the called program is realized.

Subroutine CO, the listing of which is shown in **fig. 9.5.3**, is part of the SME 800-monitor. The address is indicated either in conjunction with the system-library or by address allocation module "PUBLICS". The character, which is to be copied, is loaded in register C.

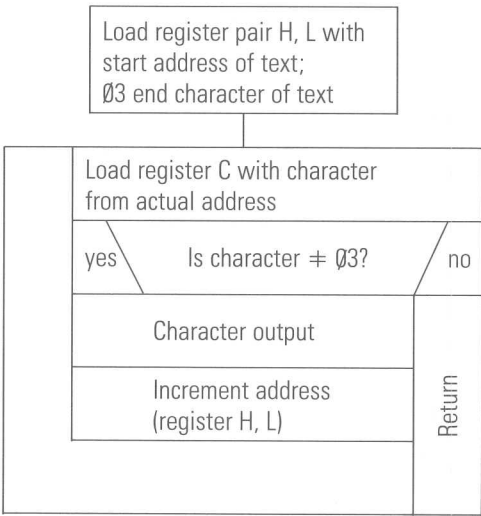


Fig. 9.5.1

ASM80 AUSG3.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0
AUSGABE VON TEXT

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	*TITLE ('AUSGABE VON TEXT')
		2	; DAS PROGRAMM GIBT EINEN TEXT AUS, DESSEN ERSTER BUCHSTABE IN DER
		3	; SPEICHERZELLE MIT ADRESSE DES INHALTES VOM REGISTERPAAR H,L STEHT.
		4	; AM ENDE DES TEXTES MUSS DAS STEUERZEICHEN 'ETX'='03H STEHEN.
		5	EXTRN C0
		6	PUBLIC AUSG3
		7	CSEG
0000	4E	8	AUSG3: MOV C,H ;
0001	3E03	9	MVI A,03H ;
0003	BE	10	CHP H ;
0004	C8	11	RZ ;
0005	CD0000	12	CALL C0 ;
0008	23	13	INX H ;
0009	C30000	14	JMP AUSG3 ;
		15	END ;

PUBLIC SYMBOLS
AUSG3 C 0000

EXTERNAL SYMBOLS
C0 E 0000

USER SYMBOLS
AUSG3 C 0000 C0 E 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.5.2

ASM80 C0.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
01E3		1	ORG 01E3H
01E3	D8FB	2	C0: IN 0FBH ;
01E5	E601	3	ANI 01H ;
01E7	CAE301	4	JZ C0 ;
01EA	79	5	MOV A,C ;
01EB	D3FA	6	OUT 0FAH ;
01ED	C9	7	RET ;
		8	END ;

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS
C0 A 01E3

ASSEMBLY COMPLETE, NO ERRORS

Fig. 9.5.3

9.6 Program for Input of Addresses and Data

The program described in the following is for input of an address, incorporating two characters, or for input of data consisting of one character. The input procedure is finished by "CR". The number of characters is loaded into register E and incorporates "CR". The first memory word address for the read characters is loaded into register pair H,L.

The address input is generally realized by loading first the two most significant hexadecimal digits and then the least significant ones. Two digits each are packed per byte. The memory word is incremented for correct loading of the two most significant digits. Thus it is guaranteed that the digit position of the address is correct loaded into the memory. After two decisions as to whether additional characters have to be loaded or the end-character "CR" had been given, the first hexadecimal number consisting of 4 digits, is shifted by four bits to left and intermediately stored as demonstrated by the structogram of **fig. 9.6.1**. The listing is shown in **fig. 9.6.2**. After input of the next character the first and the second ones are packed per byte and stored. Then the memory word address is decremented. By running in a loop the next characters can be read. These will be either the two last significant digits, if an address is read, or the end character "CR", if a data input is realized.

Register E is consequently loaded with 5 at an address input and with 3 at a code-word input.

By subroutine EING 3 the read character is output as echo, checked as to whether it is a hexadecimal number and the ASCII-code is converted to a binary one.

If too many characters or if characters, being no hexadecimal numbers, are input an error message is released. This is also the case, when an "CR" is already loaded and another number is still expected. Therefore all 4 characters for addresses and both for data have to be read as shown in the structogram of **fig. 9.6.3** and in the listing of **fig. 9.6.2**.

Used subroutines:

GETCH (Get character)

This subroutine reads a character from a console, puts the most significant bit to zero (elimination of parity sign) and transfers the character into register C as shown in structogram of **fig. 9.6.4**. The listing is indicated in **fig. 9.6.5**. The routine GETCH uses also subroutine CI. The start address is F803H for the SME 800.

VALDG (Valid digit)

Subroutine VALDG checks as to whether the read ASCII-character is a hexadecimal number or not. First it is checked whether the read value is $\geq 30H$ and then whether it is $\leq 39H$. This corresponds to figures 0 to 9. If this is not the case the check is repeated whether the input value is $\geq 41H$ or $\leq 47H$. This corresponds

to figures A to F or to decimal numbers 10 to 15. If the input value is not in the two ranges an error message is released as demonstrated in the structogram of fig. 9.6.6. The listing is shown in fig. 9.6.7.

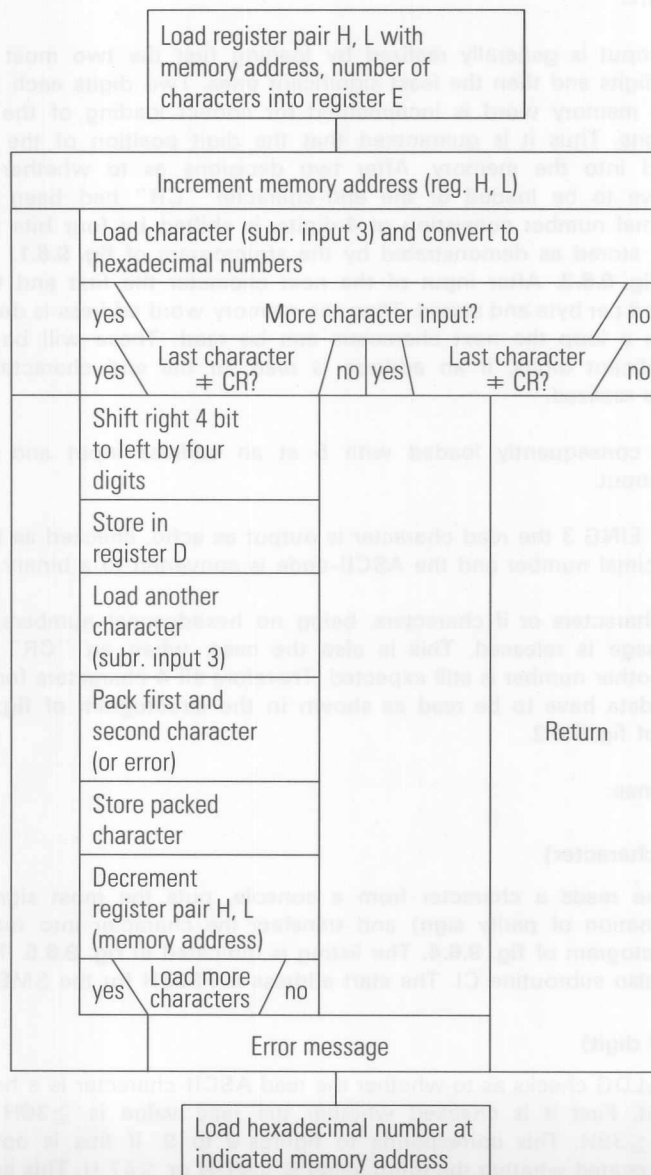


Fig. 9.6.1

LOC OBJ SEQ SOURCE STATEMENT

```

1 $TITLE ('EINGABE')
2 ; DAS PROGRAMM STEUERT DIE EINGABE EINER ANZAHL ZEICHEN. DIE
3 ; EINGABE WIRD MIT 'CR' ABGESCHLOSSEN. DIE ZEICHENZAHL WIRD IM
4 ; REGISTER E UEBERGEHEN UND SCHLIESST DAS 'CR' EIN. IM
5 ; REGISTERPAAR H,L STEHT DIE ERSTE SPEICHERADRESSE, IN DIE DIE
6 ; ZEICHEN EINGELESEN WERDEN.
7 EXTRN CNVBN
8 EXTRN CO
9 EXTRN FEHLER
10 EXTRN GETCH
11 EXTRN VALDG
12 PUBLIC EING1
13 PUBLIC WEITER
14 CSEG
0000 23 15 EING1: INX H
0001 CD0000 E 16 EING2: CALL GETCH
0004 1D 17 DCR E
0005 CA2700 C 18 JZ E1
0008 FE0D 19 CPI 0DH
000A CC0000 E 20 CZ FEHLER
000D CD2D00 C 21 CALL E2
0010 07 22 RLC
0011 07 23 RLC
0012 07 24 RLC
0013 07 25 RLC
0014 57 26 MOV D,A
0015 CD0000 E 27 CALL GETCH
0018 FE0D 28 CPI 0DH
001A CC0000 E 29 CZ FEHLER
001D CD2D00 C 30 CALL E2
0020 B2 31 ORA D
0021 77 32 MOV M,A
0022 2B 33 DCX H
0023 1D 34 DCR E
0024 C20100 C 35 JNZ EING2
0027 FE0D 36 E1: CPI 0DH
0029 C40000 E 37 CNZ FEHLER
002C C9 38 RET
002D CD0000 E 39 E2: CALL CO
0030 CD0000 E 40 CALL VALDG
0033 D20000 E 41 JNC FEHLER
0036 CD0000 E 42 WEITER: CALL CNVBN
0039 C9 43 RET
44 END

```

PUBLIC SYMBOLS

EING1 C 0000 WEITER C 0036

EXTERNAL SYMBOLS

CNVBN E 0000 CO E 0000 FEHLER E 0000 GETCH E 0000 VALDG E 0000

USER SYMBOLS

CNVBN E 0000 CO E 0000 E1 C 0027 E2 C 002D EING1 C 0000 EING2 C 0001 FEHLER E 0000
 GETCH E 0000 VALDG E 0000 WEITER C 0036

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.6.2

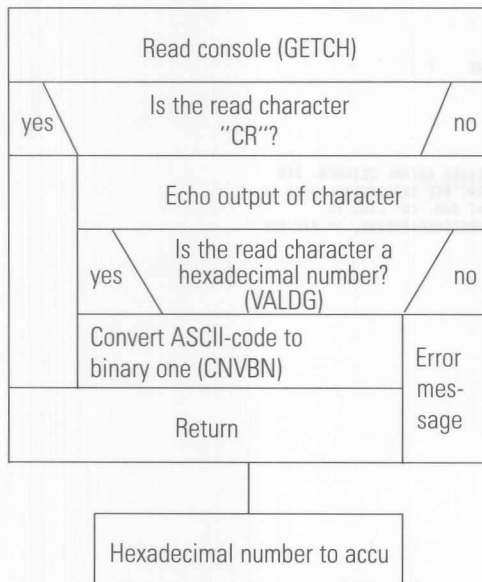


Fig. 9.6.3

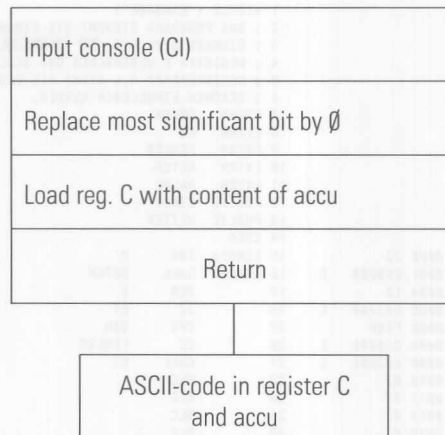


Fig. 9.6.4

ASM00 GETCH.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0

MODULE PAGE 1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	PUBLIC GETCH
		2	EXTRN CI
		3	CSEG
0000	CD0000	4	GETCH: CALL CI
0003	E67F	5	ANI 7FH
0005	4F	6	MOV C,A
0006	C9	7	RET
		8	END

PUBLIC SYMBOLS
GETCH C 0000

EXTERNAL SYMBOLS
CI E 0000

USER SYMBOLS
CI E 0000 GETCH C 0000

ASSEMBLY COMPLETE, NO ERRORS

Fig. 9.6.5

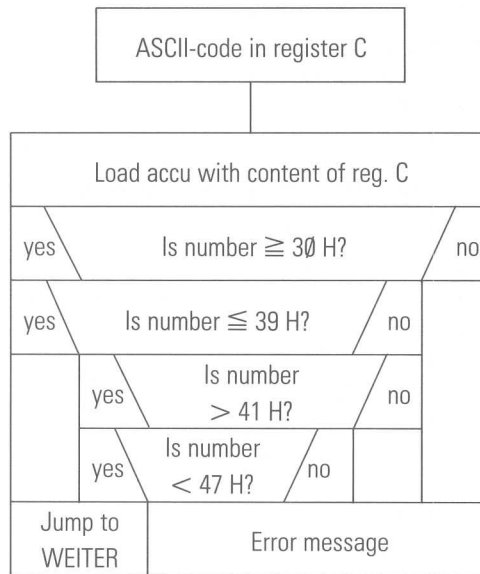


Fig. 9.6.6

ASM80 VALDG.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0

MODULE PAGE 1

LOC OBJ SEQ SOURCE STATEMENT

```

1 PUBLIC VALDG
2 EXTRN FEHLER
3 EXTRN WEITER
4 CSEG
0000 79 5 VALDG: MOV A,C
0001 FE30 6 CPI 30H
0003 FA1A00 C 7 JM FRET
0006 FE39 8 CPI 39H
0008 FA1800 C 9 JM SRET
000B CA1800 C 10 JZ SRET
000E FE41 11 CPI 41H
0010 FA1A00 C 12 JM FRET
0013 FE47 13 CPI 47H
0015 F21A00 C 14 JP FRET
0018 37 15 SRET: STC
0019 C9 16 RET
001A 37 17 FRET: STC
001B 3F 18 CMC
001C C9 19 RET
20 END

```

PUBLIC SYMBOLS
VALDG C 0000

EXTERNAL SYMBOLS
FEHLER E 0000 WEITER E 0000

USER SYMBOLS
FEHLER E 0000 FRET C 001A SRET C 0018 VALDG C 0000 WEITER E 0000

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 9.6.7

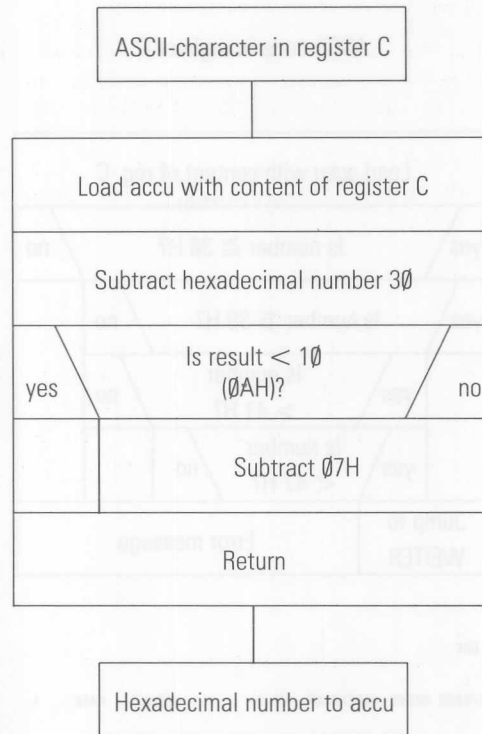


Fig. 9.6.8

```

ASH00 CNVBN.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE  PAGE 1

LOC  OBJ      SEQ      SOURCE STATEMENT

1 PUBLIC CNVBN
2 CSEG
3 CNVBN: MOV    A,C
4          SUI    30
5          CPI    10
6          RM
7          SUI    7H
8          RET
9 END

PUBLIC SYMBOLS
CNVBN C 0000

EXTERNAL SYMBOLS

USER SYMBOLS
CNVBN C 0000

ASSEMBLY COMPLETE, NO ERRORS

```

Fig. 9.6.9

CNVBN (convert to binary)

This subroutine converts the ASCII-characters to binary ones. First the hexadecimal number 30 is subtracted from the hexadecimal character and then it is checked whether the result is <10. This refers to figure 0 to 9.

If the result is not <10 the hexadecimal number 07 is again subtracted. The result is a hexadecimal figure between A and F. The structogram is shown in fig. 9.6.8 and the listing is indicated in fig. 9.6.9.

FEHLER (error message)

The listing of subroutine "FEHLER" (error message) is shown in fig. 9.6.10. First register pair H,L is loaded with the start address of text 7, which is the begin of the text "Fehlerhafte Eingabe" (incorrect input). Subroutine AUSG 3 is for text output. Then register pair H,L is loaded with the return address, being stored at memory byte RCKAD, and then its content is transferred by instruction PUSH H to the stack. The program is continued by the stored return address with the following instruction RETURN.

```
ASM80 FEHLER.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE PAGE 1
FEHLMELDUNG

LOC OBJ      SEQ      SOURCE STATEMENT

1 $TITLE ('FEHLMELDUNG')
2 PUBLIC FEHLER
3 EXTRN AUSG3
4 EXTRN TEXT7
5 EXTRN RCKAD
6 CSEG
0000 210000 E 7 FEHLER: LXI H,TEXT7 ;
0003 CD0000 E 8 CALL AUSG3 ;
0006 E1 9 POP H ;
0007 E1 10 POP H ;
0008 2A0000 E 11 LHLD RCKAD ;
000B E5 12 PUSH H ;
000C C9 13 RET ;
14 END ;

PUBLIC SYMBOLS
FEHLER C 0000

EXTERNAL SYMBOLS
AUSG3 E 0000 RCKAD E 0000 TEXT7 E 0000

USER SYMBOLS
AUSG3 E 0000 FEHLER C 0000 RCKAD E 0000 TEXT7 E 0000

ASSEMBLY COMPLETE, NO ERRORS
```

Note: For translation of the German comments pls. see preceding text.

Fig. 9.6.10

9.7 Output Program for Hexadecimal Numbers

In microcomputer systems hexadecimal numbers are generally packed by two hex-digits per byte. For output on a console a digit each has to be transferred. Besides that a conversion to ASCII-code has to be realized. The subroutine NMOUT1 is for output of a 2-digit hexadecimal number on a console.

The structogram is demonstrated in **fig. 9.7.1** and **fig. 9.7.2** shows the listing. The accu is loaded with the number. After register pair H,L, accu and flags have been written into the stack, the two half-bytes of the accu are exchanged by four rotate instructions (RRC). The most significant digit is now shifted to the least significant half-byte of the accu and vice versa. This half-byte is now masked

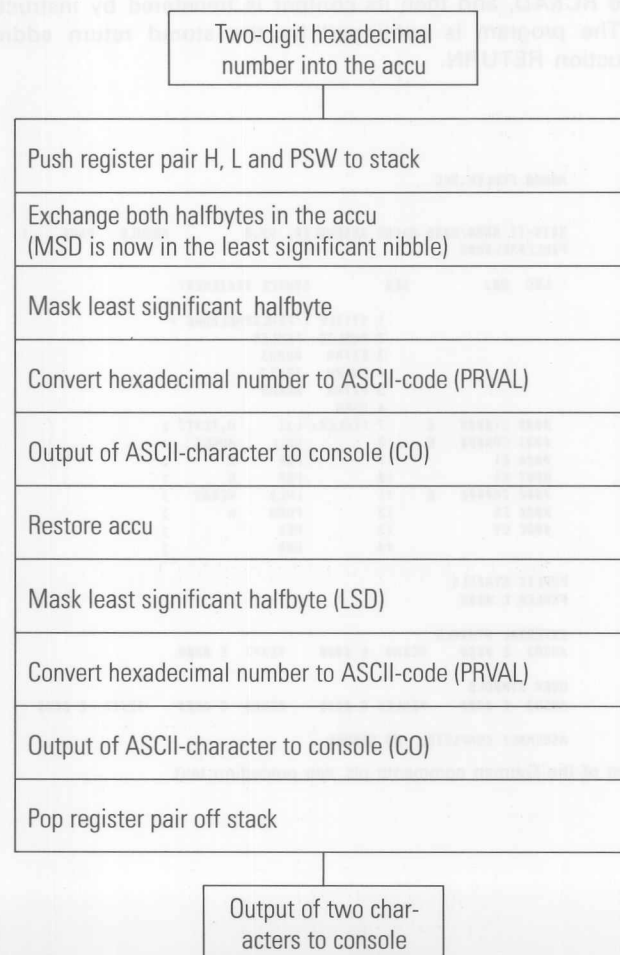


Fig. 9.7.1

LOC	OBJ	SEQ	SOURCE STATEMENT
		1	PUBLIC NMOUT
		2	EXTRN CO
		3	EXTRN PRVAL
		4	CSEG
0000	E5	5	NMOUT: PUSH H ;
0001	F5	6	PUSH PSW ;
0002	0F	7	RRC ;
0003	0F	8	RRC ;
0004	0F	9	RRC ;
0005	0F	10	RRC ;
0006	E60F	11	ANI 0FH ;
0008	4F	12	MOV C,A ;
0009	CD0000	13	CALL PRVAL ;
000C	CD0000	14	CALL CO ;
000F	F1	15	POP PSW ;
0010	E60F	16	ANI 0FH ;
0012	4F	17	MOV C,A ;
0013	CD0000	18	CALL PRVAL ;
0016	CD0000	19	CALL CO ;
0019	E1	20	POP H ;
001A	C9	21	RET ;
		22	END

PUBLIC SYMBOLS

NMOUT C 0000

EXTERNAL SYMBOLS

CO E 0000 PRVAL E 0000

USER SYMBOLS

CO E 0000 NMOUT C 0000 PRVAL E 0000

ASSEMBLY COMPLETE, NO ERRORS

Fig. 9.7.2

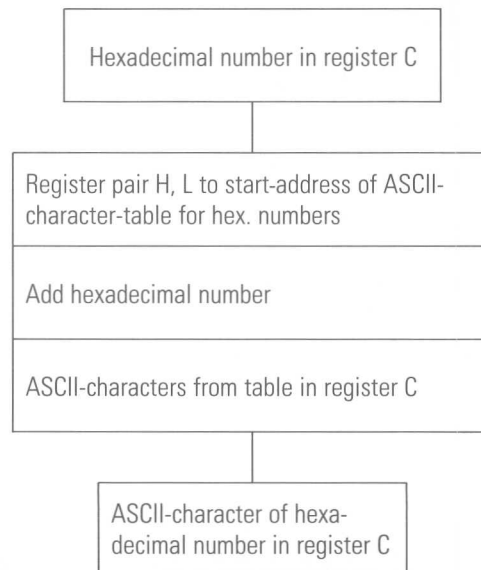


Fig. 9.7.3

and the hexadecimal number is converted to ASCII-code by subroutine PRVAL1. The ASCII-character is transferred to the console by subroutine CO, as shown in fig. 9.5.3. Then the original number is moved from the stack to the accu, the least significant half-byte is masked, converted to a hexadecimal number and transferred to the console. By restoring register pair H,L the original program is now continued.

PRVAL1 (print value)

The subroutine PRVAL1 is shown in **fig. 9.7.3** and **fig. 9.7.4**. It converts a hexadecimal number of the register C to an ASCII-character by using an ASCII-conversion table. The register pair H,L is loaded with the start address of this conversion table and the hexadecimal number, which is to be displayed, is added. Register pair H,L contains now the address of the character which is to be displayed. The instruction MOV C,M loads the ASCII-character into register C. Then it is transferred to the console by subroutine CO (see fig. 9.5.3).

The start address for subroutine CO is F809H, if an SME 800 is used.

```

ASM80 PRVAL1.SRC

ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0      MODULE PAGE 1

LOC OBJ      SEQ      SOURCE STATEMENT

          1 PUBLIC  PRVAL
          2 CSEG
0000 210800  C      3 PRVAL: LXI    H,DIGTB ;
0003 0600          4          MVI    B,0  ;
0005 09          5          DAD     B    ;
0006 4E          6          MOV    C,H   ;
0007 C9          7          RET
0008 30313233     8 DIGTB: DB      '0123456789ABCDEF'
000C 34353637
0010 38394142
0014 43444546

          9 END

PUBLIC SYMBOLS
PRVAL C 0000

EXTERNAL SYMBOLS

USER SYMBOLS
DIGTB C 0000 PRVAL C 0000

ASSEMBLY COMPLETE, NO ERRORS

```

Fig. 9.7.4

10. Applications with Microcomputer System SAB 8048

10.1 Hard- and Software for Operating A/D-Converter SAB 3060 P in Conjunction with SAB 8748

An analog/digital-converter is required, if analog sensor signals have to be processed by a microcomputer system. In the following three different programs for operating the Siemens 8-bit A/D-converter SAB 3060 P in conjunction with the microcomputer SAB 8748 are described.

Circuit and program

As demonstrated in **fig. 10.1.1** the data outputs of SAB 3060 P are directly connected to the microcomputer data bus DB 0 to DB 7. The clock signal for the A/D-converter is available at pin T0 of the SAB 8748. The frequency of the crystal oscillation is internally divided by a factor of 3, i.e. when the microcomputer is operated at 6 MHz a clock signal with a frequency of 2 MHz is available at T0.

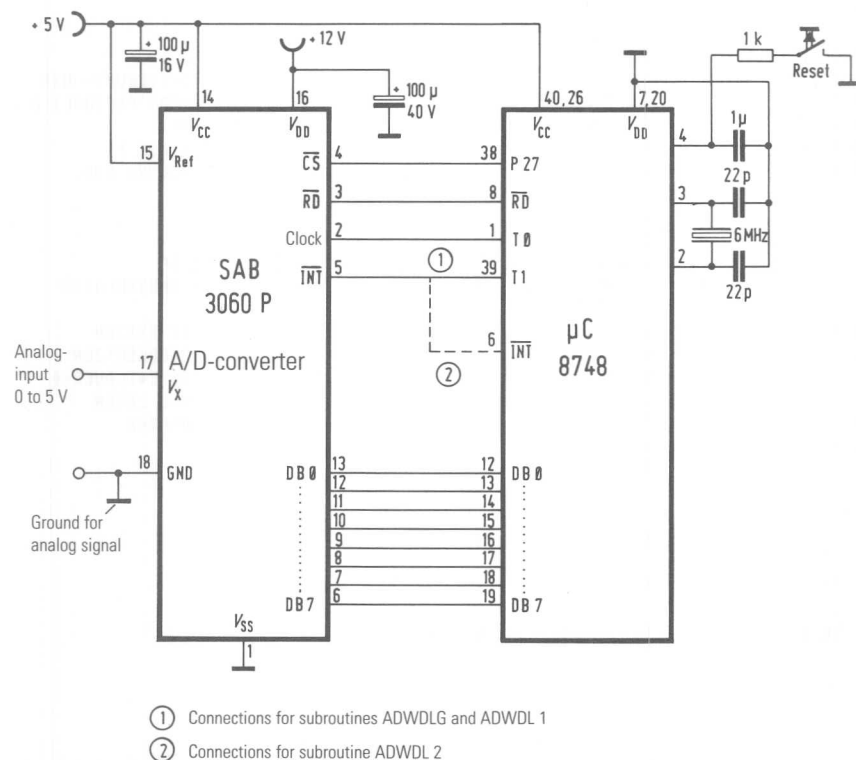


Fig. 10.1.1

The output signal $\overline{\text{INT}}$ of the SAB 3060 P is supplied to T1 of the microcomputer. Pins $\overline{\text{RD}}$ of both devices are directly connected. For chip selection ($\overline{\text{CS}}$) a signal is available at pin P27 of the microcomputer.

The program listing is shown in **fig. 10.1.2**. By the first instruction ENT0 CLK the signal at pin T0 is applied to the buffer stage of the clock output. The following jump instruction guarantees a free memory for interrupt vector and timer interrupt vector. Then subroutine ADWDLG is called. It organizes the polling of the A/D-converter. The data is stored in the accumulator. It is processed by instruction OUTL P1,A and available at port 1, to which a display can be connected.

Instruction JMP START closes the loop for a cyclic polling, if no other operations have to be processed by the microcomputer.

ASM48 TEST1.SRC

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0

PAGE 1

LOC	OBJ	LINE	SOURCE STATEMENT
0000	75	1	ENT0 CLK ;TAKT AUF T0 LEGEN
0001	040A	2	JMP START ;ADRESSRAUM FUEER INTERRUPT- UND
000A		3	ORG 0AH ;TIMERINTERRUPTVEKTOR FREIHALTEN
000A	140F	4	START: CALL ADWDLG ;ABFRAGE AD-WANDLER
000C	39	5	OUTL P1,A ;WANDLUNGSEERGBNIS AUF P1
000D	040A	6	JMP START ;ZYKLISCHE WIEDERHOLUNG BZW.
		7	
		8	
		9	*INCLUDE(ADWDLG.SRC)
		= 10	;UNTERPROGRAMM 'ADWDLG' FRAGT DEN AD-WANDLER
		= 11	;SAB 3060 AB UND GIBT DEN MESSWERT AN DEN AKKUMULATOR
		= 12	;CHIP-SELECT = P27
000F	9A7F	= 13	ADWDLG: ANL P2,#7FH ;CHIP-SELECT SETZEN
0011	80	= 14	MOVX A,@R0 ;INT-QUER RUECKSETZEN
0012	5612	= 15	WDLG: JTI WDLG ;WARTEN, BIS INT-QUER=0
0014	08	= 16	INS A,BUS ;WERT IN AKKU LESEN
0015	8A80	= 17	ORL P2,#80H ;CHIP ABSCHALTEN
0017	83	= 18	RET
		19	END

USER SYMBOLS
ADWDLG 000F START 000A WDLG 0012

ASSEMBLY COMPLETE, NO ERRORS

Fig. 10.1.2 Listing of subroutine ADWDLG

Subroutine ADWDLG

Instruction ANL P2,#7FH at the symbolic address ADWDLG applies L-level to pin P27 and thus the A/D-converter SAB 3060 P is selected. The following instruction MOVX A, R0 has two functions. First the data bus of the microcomputer is set to high-impedance state, second an $\overline{RD}$ -pulse is released in that the $\overline{INT}$ -signal of the SAB 3060 P is reset, when a conversion result is available in the output register. It is insignificant for this instruction what the actual content of register R0 is. In this case the data, being transferred from the accumulator, is later overwritten. A new conversion is started by the A/D-converter at the end of the $\overline{RD}$ -pulse ($\overline{RD} \triangleq H$). This intentional measure guarantees that the latest result of the analog input is always polled when subroutine ADWDLG is called. Now the A/D-converter requires 84 clock cycles for the conversion, i.e. the result is not available before 42 μs have passed. If there is no conversion result, the $\overline{RD}$ -pulse is ineffective for the SAB 3060 P, as a new conversion is just running.

An L-level at $\overline{INT}$ indicates that a conversion result is available from the output register. By instruction JT1 WDLG the microcomputer checks as to whether its input T1 has H-level or not. As long as there is an H-level a conversion result is still not available.

The microcomputer continues its program at symbolic address WDLG, i.e. it remains in the loop of this symbolic address. When $\overline{INT}$ changes to L-level, the program can be continued and by the next instruction INSA,BUS the conversion result is transferred from output register to accumulator. Now the device is cut off by instruction ORL P2,#80H, i.e. pin P27 has H-level. By the next instruction RET a return to the main program is achieved.

In the described application the subroutine is characterized by the fact in that the latest result of the analog input is always read by the microcomputer. The program runs approx. 70 μs (at 6 MHz-crystal).

Subroutine ADWDL1

Another solution can be obtained by polling the A/D-converter as to whether a new conversion result is available since the last reading or not. If "yes" this result is immediately stored in a RAM-address. If no result is available, the subroutine is immediately left and the main program continues. This second solution is advantageously applied when no waiting is desired by the main program. In this case the subroutine has to be modified as demonstrated in **fig. 10.1.3**.

By the first instruction test point T1 is polled as to whether H-level is available or not (i.e. a new conversion result is not available). If there is H-level the subroutine immediately jumps to the symbolic address RETURN, which contains instruction RET. Thus a return to the main program is realized.

If a new conversion result is indicated by an L-level at test point T1, the following instruction ANL P2,#7FH sets pin P27 to L-level and selects the IC SAB 3060 P. By instruction MOVX A,@R0 the conversion result is transferred to the accumulator. The following instruction MOV@R0,A moves this result to a RAM byte, which

LOC	OBJ	LINE	SOURCE STATEMENT
0000	75	1	ENT0 CLK ;TAKT AUF T0 LEGEN
0001	040A	2	JMP START ;ADRESSRAUM FUER INTERRUPT- UND
000A		3	ORG 0AH ;TIMERINTERRUPTVEKTOR FREIHALTEN
000A	8827	4	START: MOV R0,#27H ;ADRESSIERUNG DES ZWISCHENSPEICHERS
000C	1412	5	CALL ADWDL1 ;ABFRAGE AD-WANDLER OB NEUE DATEN
000E	F0	6	MOV A,0R0 ;ZWISCHENSPEICHER IN AKKU
000F	39	7	OUTL P1,A ;WANDLUNGSERGEBNIS AUF P1
0010	040A	8	JMP START ;ZYKLISCHE WIEDERHOLUNG BZW.
		9	;HIER WEITERES PROGRAMM
		10	
		11	
		12	*INCLUDE(ADWDL1.SRC)
		= 13	;UNTERPROGRAMM 'ADWDL1' FRAGT DEN AD-WANDLER SAB 3060 AB UND
		= 14	;GIBT DEN MESSWERT IN DIE MIT R0 ADRESSIERTE SPEICHERSTELLE.
		= 15	;CHIP-SELECT = P27
0012	561A	= 16	ADWDL1: JT1 RETURN ;RETURN, WENN KEIN WANDLUNGSERGEBNIS
0014	9A7F	= 17	ANL P2,#7FH ;CHIP-SELECT SETZEN
0016	80	= 18	MOVX A,0R0 ;WERT IN AKKU LESEN
0017	A0	= 19	MOV 0R0,A ;WERT IN RAM-SPEICHER
0018	8A80	= 20	ORL P2,#80H ;CHIP ABSCHALTEN
001A	83	= 21	RETURN: RET
		22	END

USER SYMBOLS

ADWDL1 0012 RETURN 001A START 000A

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.1.3 Listing for subroutine ADWDL1

is addressed by the content of register R0. The next instruction ORL P2,#80H sets pin P27 to H-level. A conversion start was already released at the leading edge of the $\overline{RD}$ -signal with instruction MOVXA,@R0. By instruction RET a return to the main program is now realized.

Before this subroutine is called, the main program has to indicate the memory address, where the conversion result of the A/D-converter is to be stored, by content of register R0. The access time of the subroutine shown in fig. 10.1.3 is 27.5 μ s (at 6 MHz-crystal) assuming that a conversion is always available. Without conversion result the program of fig. 10.1.3 runs 7.5 μ s.

Polling of A/D-converter via interrupt

In this case $\overline{INT}$ of SAB 3060 P is connected to $\overline{INT}$ of the microcomputer. In the main program shown in **fig. 10.1.4** a jump instruction for subroutine ADWDL2 is stored at the interrupt vector (address 0003). As register R0 can have any

content when the main program is interrupted, it has preferably to be loaded with the desired memory address by the subroutine, in this case 27H (see listing of fig. 10.1.4). Register bank 1 is previously selected by SEL RB1 to avoid that the register-R0-data of register bank 0 is not destroyed. Polling of pin T1 is not necessary as the program is always interrupted when a new conversion result is available.

The other instructions are the same as shown in the listing of fig. 10.1.3. However, in this case the return instruction RETR is utilized. It sets bits 4 to 7 of the program status word, and thus also the register bank, to the old status (before interrupt).

The A/D-converter has to be started when the microcomputer is turned on, otherwise the conversion is not started, i.e. $\overline{\text{INT}}$ has not L-level and thus no interrupt is released. The start is achieved by instruction CALL ADWDL2. As by instruction MOVX A,@R0 of the subroutine a conversion result of the A/D-converter cannot

ASH48 TEST02.SRC

ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, V3.0

PAGE 1

LOC	OBJ	LINE	SOURCE STATEMENT
0000	75	1	ENT0 CLK ;TAKT AUF T0 LEGEN
0001	040A	2	JMP START ;HAUPTPROGRAMM AUSFUEHREN
0003		3	ORG 03H ;INTERRUPTVEKTOR
0003	0413	4	JMP ADWDL2 ;ABFRAGE AD-WANDLER
000A		5	ORG 0AH ;TIMERINTERRUPTVEKTOR FREIHALTEN
000A	1413	6	START: CALL ADWDL2 ;STARTEN DER 1.AD-WANDLUNG
000C	05	7	WDHOLE: EN I ;INTERRUPT FREIGEBEN
000D	B827	8	MOV R0,#27H ;ADRESSIERUNG ZWISCHENSPEICHER
000F	F0	9	MOV A,@R0 ;ZWISCHENSPEICHER IN AKKU
0010	39	10	OUTL P1,A ;WANDLUNGSERGEBNIS AUF P1
0011	040C	11	JMP WDHOLE ;ZYKLISCHE WIEDERHOLUNG BZW.
		12	;HIER WEITERES PROGRAMM
		13	
		14	
		15	
		16	\$INCLUDE(ADWDL2.SRC)
		= 17	;UNTERPROGRAMM 'ADWDL2' FRAGT DEN AD-WANDLER SAB 3060 AB UND
		= 18	;GIBT DEN MESSWERT IN DIE RAM-SPEICHERSTELLE 27H AUS.
		= 19	;CHIP-SELECT = P27
0013	D5	= 20	ADWDL2: SEL RB1 ;REGISTERBANK 1 ANWAEGHEN
0014	B827	= 21	MOV R0,#27H ;SPEICHERSTELLE ADRESSIEREN
0016	9A7F	= 22	ANL P2,#7FH ;CHIP-SELECT SETZEN
0018	80	= 23	MOVX A,@R0 ;WERT IN AKKU LESEN
0019	A0	= 24	MOV @R0,A ;WERT IN RAM-ZWISCHENSPEICHER
001A	8A80	= 25	ORL P2,#80H ;CHIP ABSCHALTEN
001C	93	= 26	RETR ;RETURN MIT RESTORE PSW
		27	END

USER SYMBOLS

ADWDL2 0013 START 000A WDHOLE 000C

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.1.4 Listing of subroutine ADWDL2

be available, an undefined value is intermediately stored at the memory address for the first time (in this case #27H). The conversion time is approx. 42 μ s.

If this start procedure is to be avoided the two instructions

ANL P2,#7FH and

ORL P2,#80H

have to be used instead of CALL ADWDL2.

In the main program external interrupts can be ignored by instruction DIS I. This is especially required when the content of the accumulator is not to be destroyed by an interrupt subroutine. If a new conversion result of the A/D-converter is required, an interrupt is enabled by the main program instruction EN I.

Before the memory byte (in this case #27H) is read, register R0 is to be loaded with its address, because register R0 of register bank RB1 had been used by the subroutine.

Advantages and disadvantages of the three described subroutines

- a) ADWDLG: The subroutine releases a new conversion start. The advantage is in that the latest analog value is available.
The disadvantage is in that the subroutine has an access time which is always as long as the conversion time of the A/D-converter.
- b) ADWDL1: The subroutine is immediately left when a conversion result is not available.
Advantage: Access time optimum.
Disadvantage: With longer main programs the conversion result can not be the latest one.
- c) ADWDL2: The intermediate memory is always overwritten by the latest conversion result when an interrupt occurs.
Advantage: Access time optimum.
Disadvantage: The main program is often interrupted.
For another interrupt additional hard- and software are required.

Components for circuit 10.1

			Ordering code
1 8-bit single-chip micro-computer (6-MHz-version)	SAB 8048-D		Q67120-C37-D88
1 8-bit-analog-digital-converter	SAB 3060-P		Q67120-P53
2 Polypropylene capacitors	22 pF/630 V		B33063-B6220-F
1 Tantalum capacitor	1 μ F/40 Vdc		B45181-B4105-M
2 Alu-electrolytic capacitors	100 μ F/16 Vdc (+50, -10%)		B41588-C4107-T
1 Carbon layer resistor	1 k Ω , 0.5 W, $\pm$ 5%		B51261-Z4102-J1
1 Crystal	6 MHz		—

10.2 Display Panel with LCD-Module LCM 1001

The display panel utilizing the LCD-module LCM 1001 is specified for twelve 4-digit displays with the size of DIN A 4-format. They are mounted in two columns of 6 devices each. Every display can be selected, set and reset by the key board. An input has to be acknowledged by operating a special acknowledgement key. The key board uses simple push buttons with make-contacts. They do not have any code generator.

The control circuit is shown in **fig. 10.2.1**. The nucleus of this circuit is the single-chip MC SAB 8748 which can be programmed by the user. The IC SAB 8243 is for I/O-expansion. Besides the decoders, type 4514, for display selection and the gate-ICs, type 4081, a monostable multivibrator IC, type 4047, is only required for generating the interrupt enable pulse. Four buffer stages, type 4050, are necessary for driving the key board matrix (see **fig. 10.2.2**).

Program

The structogram for the program is indicated in **fig. 10.2.3** and **fig. 10.2.4** shows the listing.

A reset is automatically obtained after the supply voltage is applied, i.e. the displays are reset. Leading zeros are suppressed. The circuit operates in a waiting loop as long as an interrupt is requested.

After operating one of the push buttons the matrix columns are successively activated (high level) and the lines are sequentially scanned. Register 1 stores the figure corresponding to the operated push button. Thereafter this information is transferred to the display register 4. This intermediate storing is necessary because it has to be checked as to whether register 4 is empty or not. In the latter case the content has to be shifted in a higher significant register.

In the following a decision has to be made whether a display addressing (column A or B) or a writing of another figure is to be realized with the next push button scanning.

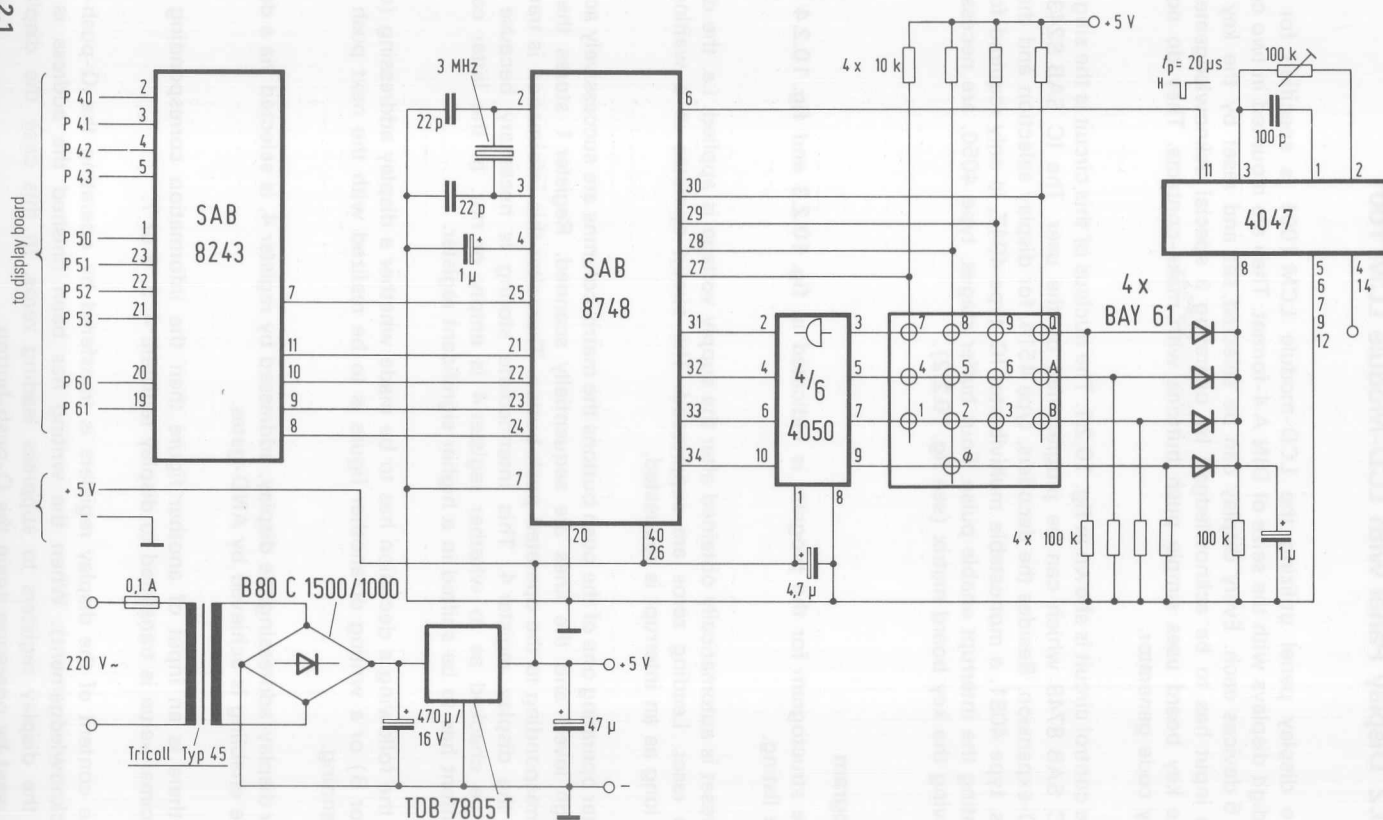
For display-addressing the display, addressed by register 4, is selected via a decoder. The enabling is achieved by AND-gates.

If there is an input of another figure then the information corresponding to the decimal value is transferred to display registers 4, 5, 6 or 7.

The content of the display registers is transferred by operating the Q-push-button (acknowledgement). When the writing has been finished the address is stored in the display registers to suppress leading zeros. In this case the display can be reset by operating again the Q-push-button.

Fig. 10.2.1

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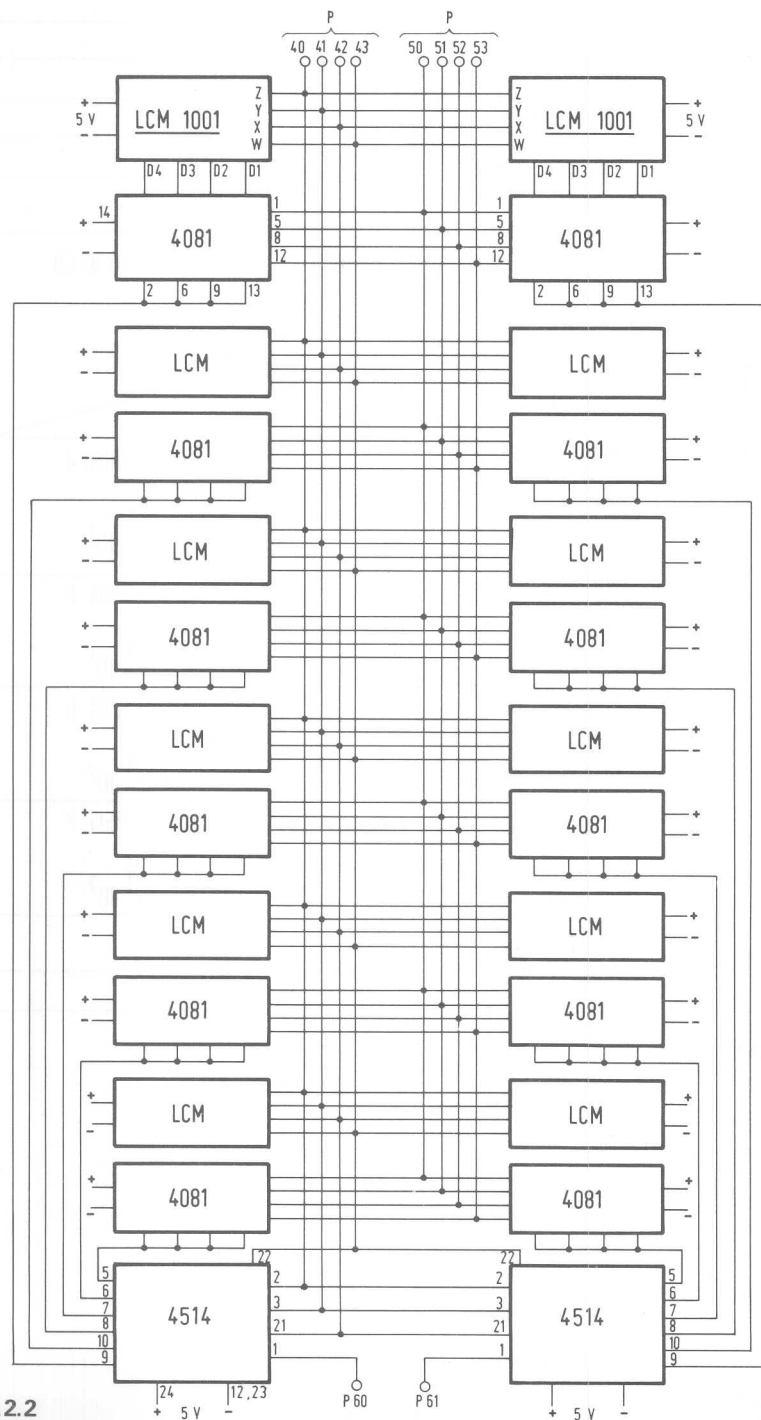


Fig. 10.2.2

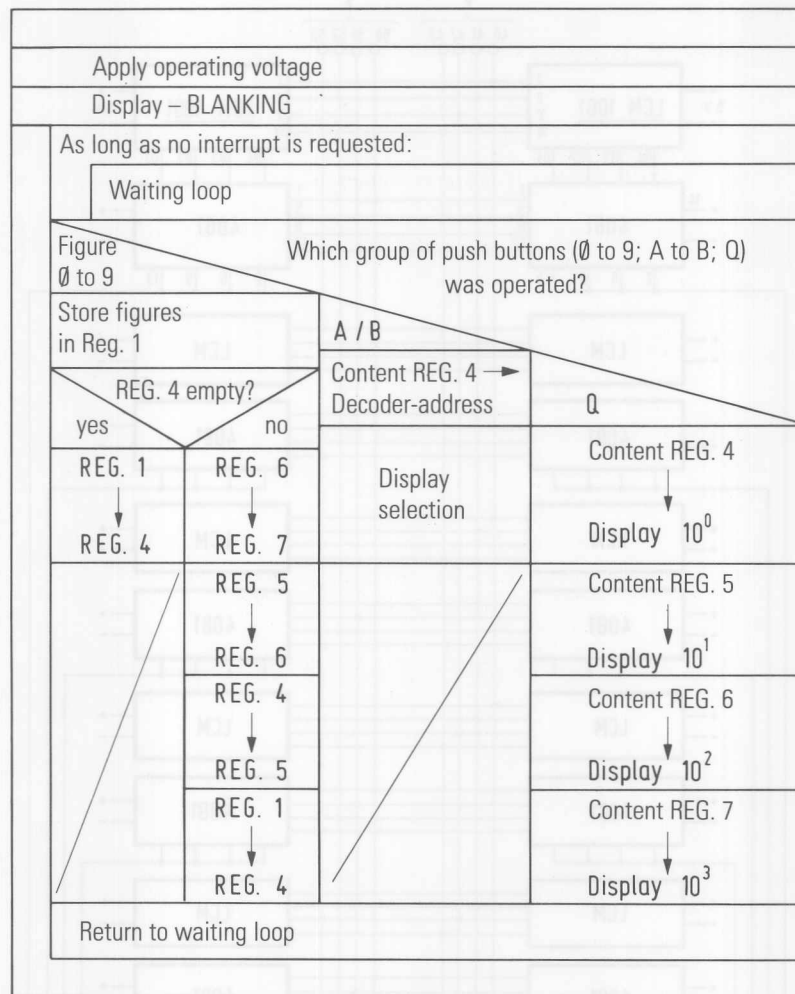


Fig. 10.2.3

LOC	OBJ	LINE	SOURCE STATEMENT
		1	;***** ANZEIGETAFEL *****
		2	;BESCHREIBEN VON ZWOLF 4-STELLIGEN LCD-ANZEIGE-MODULEN
		3	;UEBER EINGABETASTATUR .
		4	;EDITOR:B AT SE (LINDL)
		5	;
		6	;
		7	;
0000		8	ORG 0000H ;START-ADRESSE
0000 0410		9	JMP ANFG
0003		10	ORG 0003H ;INTERRUPTVEKTOR-ADRESSE
0003 0417		11	JMP ARBEIT
0010		12	ORG 0010H
0010 14FE		13	ANFG: CALL CLEAR ;DISPLAY-BLANK
0012 89FF		14	WART: ORL P1,0FFH ;SPALTEN,ZEILEN HIGH
0014 05		15	EN I
0015 0412		16	JMP WART ;WARTESCHLEIFE,BIS INTERRUPT-AUFFORDERUNG ERFOLGT
		17	\$EJECT

Fig. 10.2.4 (Page 1)

LOC	OBJ	LINE	SOURCE STATEMENT
		18	;ABFRAGE DER ZEILENMATRIX UND TRANSFER DES DEM TASTENAUFTRUF
		19	;ENTSPRECHENDEN ZEICHENS IN DIE ANZEIGEREGISTER R4,5,6,7.
0017 B5		20	ARBEIT: CLR F0 ;FLAG 0 RUECKSETZEN
0018 23F1		21	MOV A,0F1H
001A 39		22	OUTL P1,A ;SPALTE 1 AKTIVIERT
001B 09		23	IN A,P1 ;PORT 1 FUEH ZEILENABFRAGE IN AKKU
001C F7		24	RLC A ;BIT 7 IN UEBERTRAG
001D F7		25	RLC A ;BIT 6 IN UEBERTRAG
001E F6DA		26	JC ZIF1 ;WENN CB =1 ZIF1 IN ANZEIGEREGISTER
0020 F7		27	RLC A ;BIT 5 IN UEBERTRAG
0021 F6E6		28	JC ZIF4
0023 F7		29	RLC A
0024 F6F2		30	JC ZIF7
0026 23F2		31	MOV A,0F2H
0028 39		32	OUTL P1,A ;SPALTE 2 AKTIVIERT
0029 09		33	IN A,P1
002A F7		34	RLC A
002B F6D6		35	JC ZIF0
002D F7		36	RLC A
002E F6DE		37	JC ZIF2
0030 F7		38	RLC A
0031 F6EA		39	JC ZIF5
0033 F7		40	RLC A
0034 F6F6		41	JC ZIF8
0036 23F4		42	MOV A,0F4H ;SPALTE 3 AKTIVIERT
0038 39		43	OUTL P1,A
0039 09		44	IN A,P1
003A F7		45	RLC A
003B F7		46	RLC A
003C F6E2		47	JC ZIF3
003E F7		48	RLC A
003F F6EE		49	JC ZIF6
0041 F7		50	RLC A
0042 F6FA		51	JC ZIF9
0044 23F8		52	MOV A,0F8H
0046 39		53	OUTL P1,A ;SPALTE 4 AKTIVIERT
0047 09		54	IN A,P1
0048 F7		55	RLC A
0049 F7		56	RLC A
004A F674		57	JC ZIFB ;AUFRUF DISPLAYREIHE B
004C F7		58	RLC A
004D F667		59	JC ZIFA ;AUFRUF DISPLAYREIHE A
004F F7		60	RLC A
0050 F681		61	JC QITTU ;WENN CB =1,INH.ANZ6.-REG. IN DISPLAY EINSCHREIBEN
0052 93		62	RETR ;RUECKSPRUNG IN WARTESCHLEIFE
		63	\$EJECT

Fig. 10.2.4 (Page 2)

LOC	OBJ	LINE	SOURCE STATEMENT
		64	;ANZEIGEREGISTER-ZURUECKSETZEN (=ANZEIGE-BLANK)
0053	BF0F	65	BLANK: MOV R7,#0FH
0055	BE0F	66	MOV R6,#0FH
0057	BD0F	67	MOV R5,#0FH
0059	BC0F	68	MOV R4,#0FH
005B	83	69	RET
		70	;
		71	;POSITIONSDEKODER RUECKSETZEN.
005C	2300	72	DEKRES: MOV A,#00H
005E	3C	73	MOVD P4,A
005F	3E	74	MOVD P6,A
0060	230F	75	MOV A,#0FH
0062	3E	76	MOVD P6,A
0063	2300	77	MOV A,#00H
0065	3E	78	MOVD P6,A
0066	83	79	RET
0067	145C	80	ZIFA: CALL DEKRES
0069	FC	81	MOV A,R4
006A	3C	82	MOVD P4,A ;ANWAHL DES GEWUENSCHTEN DISPLAYS (DATEN)
006B	2301	83	MOV A,#01H
006D	3E	84	MOVD P6,A ;DEKODER AKTIVIEREN (REIHE A)
006E	2300	85	MOV A,#00H
0070	3E	86	MOVD P6,A
0071	1453	87	CALL BLANK
0073	93	88	RETR
0074	145C	89	ZIFB: CALL DEKRES
0076	FC	90	MOV A,R4
0077	3C	91	MOVD P4,A
0078	2302	92	MOV A,#02H
007A	3E	93	MOVD P6,A
007B	2300	94	MOV A,#00H
007D	3E	95	MOVD P6,A
007E	1453	96	CALL BLANK
0080	93	97	RETR
		98	\$EJECT

Fig. 10.2.4 (Page 3)

LOC	OBJ	LINE	SOURCE STATEMENT
		99	;UEBERNAHME DER ANZEIGEREGISTER-INHALTE IN DIE
		100	;DISPLAY-SPEICHER
0081	FC	101	QUITU: MOV A,R4
0082	3C	102	MOVD P4,A ;DATEN AUS REG.4 AUF DATENLEITUNG P4 GEBEN
0083	2301	103	MOV A,#01H
0085	3D	104	MOVD P5,A ;EINSCHREIBEN IN DIGIT 1
0086	00	105	NOP ;SCHREIBIMPULSVERLÄNGERUNG
0087	2300	106	MOV A,#00H
0089	3D	107	MOVD P5,A ;RESET SCHREIBIMPULS
008A	FD	108	MOV A,R5
008B	3C	109	MOVD P4,A
008C	2302	110	MOV A,#02H
008E	3D	111	MOVD P5,A ;EINSCHREIBEN IN DIGIT 2
008F	00	112	NOP
0090	2300	113	MOV A,#00H
0092	3D	114	MOVD P5,A
0093	FE	115	MOV A,R6
0094	3C	116	MOVD P4,A
0095	2304	117	MOV A,#04H
0097	3D	118	MOVD P5,A ; " " " " 3
0098	00	119	NOP
0099	2300	120	MOV A,#00H
009B	3D	121	MOVD P5,A
009C	FF	122	MOV A,R7
009D	3C	123	MOVD P4,A
009E	2308	124	MOV A,#08H ; " " " " 4
00A0	3D	125	MOVD P5,A
00A1	00	126	NOP
00A2	2300	127	MOV A,#00H
00A4	3D	128	MOVD P5,A
00A5	B6D3	129	JF0 CA ;WENN F0 GESETZT, INCR.REG3 UND FORTSETZ. CLEAR
00A7	1453	130	CALL BLANK
00A9	93	131	RETR ;RET. WARTESCHLEIFE
		132	\$EJECT

Fig. 10.2.4 (Page 4)

LOC	OBJ	LINE	SOURCE STATEMENT
		133	;ORDNEN DER EINGEGEBENEN ZAHLEN IN DEN ANZEIGEREGISTERN
00AA	FC	134	NUME: MOV A,R4 ;INHALT REGISTER 4 IN AKKU
00AB	F7	135	RLC A ;BIT 7 IN UEBERTRAG
00AC	E6BB	136	JNC TA ;WENN CB=1,DANN REG.1 CHANGE REG.4
00AE	FD	137	MOV A,R5 ;INHALT REG.5 IN AKKU
00AF	F7	138	RLC A
00B0	E6BE	139	JNC TB
00B2	FE	140	MOV A,R6
00B3	F7	141	RLC A
00B4	E6C3	142	JNC TC
00B6	FF	143	MOV A,R7
00B7	F7	144	RLC A
00B8	E6CA	145	JNC TD
00BA	93	146	RETR
00BB	F9	147	TA: MOV A,R1
00BC	2C	148	XCH A,R4
00BD	93	149	RETR
00BE	FC	150	TB: MOV A,R4
00BF	2D	151	XCH A,R5
00C0	F9	152	MOV A,R1
00C1	2C	153	XCH A,R4
00C2	93	154	RETR
00C3	FD	155	TC: MOV A,R5
00C4	2E	156	XCH A,R6
00C5	FC	157	MOV A,R4
00C6	2D	158	XCH A,R5
00C7	F9	159	MOV A,R1
00C8	2C	160	XCH A,R4
00C9	93	161	RETR
00CA	FE	162	TD: MOV A,R6
00CB	2F	163	XCH A,R7
00CC	FD	164	MOV A,R5
00CD	2E	165	XCH A,R6
00CE	FC	166	MOV A,R4
00CF	2D	167	XCH A,R5
00D0	F9	168	MOV A,R1
00D1	2C	169	XCH A,R4
00D2	93	170	RETR
00D3	1B	171	CA: INC R3
00D4	2402	172	JMP CC
		173	\$EJECT

Fig. 10.2.4 (Page 5)

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LOC  OBJ      LINE      SOURCE STATEMENT
174 ;EINSCHREIBEN DER DEM TASTENAUFTRUF ENTSPRECHENDEN ZIFFERN
175 ;0 - 9 IN DAS ANZEIGEREGISTER R1,WOBEI DIE VOR DEM HEXZIFFERN-
176 ;WERT STEHENDEN ' 8 ' ZUR KONTROLLE DER REGISTERBELEGUNG
177 ;BENÖTIGT WIRD.
00D6 B980      178 ZIF0:  MOV R1,#00H
00D8 04AA      179      JMP NUME
00DA B981      180 ZIF1:  MOV R1,#01H
00DC 04AA      181      JMP NUME
00DE B982      182 ZIF2:  MOV R1,#02H
00E0 04AA      183      JMP NUME
00E2 B983      184 ZIF3:  MOV R1,#03H
00E4 04AA      185      JMP NUME
00E6 B984      186 ZIF4:  MOV R1,#04H
00E8 04AA      187      JMP NUME
00EA B985      188 ZIF5:  MOV R1,#05H
00EC 04AA      189      JMP NUME
00EE B986      190 ZIF6:  MOV R1,#06H
00F0 04AA      191      JMP NUME
00F2 B987      192 ZIF7:  MOV R1,#07H
00F4 04AA      193      JMP NUME
00F6 B988      194 ZIF8:  MOV R1,#08H
00F8 04AA      195      JMP NUME
00FA B989      196 ZIF9:  MOV R1,#09H
00FC 04AA      197      JMP NUME
198      ;
199 ;MIT CLEAR WERDEN IN 6 SCHRITTEN ALLE ANZEIGEN GEBLANKT.
00FE B801      200 CLEAR: MOV R3,#01H ;DATEN ZUR ANWAHL DER ANZEIGEN IN REIHE1 EINGEBEN
0100 B807      201      MOV R0,#07H ;EINGABE POSITIONSREGISTER(=6 DISPLAYREIHEN)
0102 FB        202 CC:    MOV A,R3
0103 3C        203      MOVD P4,A ;DATEN AN DEKODER
0104 2300      204      MOV A,#00H
0106 3E        205      MOVD P6,A
0107 2303      206      MOV A,#03H ;DEKODER (A,B) AKTIVIEREN
0109 3E        207      MOVD P6,A
010A 2300      208      MOV A,#00H
010C 3E        209      MOVD P6,A
010D C8        210      DEC R0 ;POSITIONSREGISTER(R0) DEKREMENTIEREN
010E F8        211      MOV A,R0
010F 9612      212      JNZ CB ;WENN INHALT R0 = 1,SPRUNG NACH CB
0111 83        213      RET
0112 1453      214 CB:    CALL BLANK ;ANZEIGEREGISTER RUECKSETZEN
0114 85        215      CLR F0
0115 95        216      CPL F0 ;FLAG 0 SETZEN!(VERHINDERT RUECKSPRUNG IN
217      ;WARTESCHLEIFE BEI QITTU)
0116 0481      218      JMP QITTU ;ANZEIGEN WERDEN IN QITTU GEBLANKT
219      END

```

USER SYMBOLS

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ANFG 0010  ARBEIT 0017  BLANK 0053  CA 00D3  CB 0112  CC 0102  CLEAR 00FE  DEKRES 005C
NUME 00AA  QITTU 0001  TA 00BB  TB 00BE  TC 00C3  TD 00CA  WART 0012  ZIF0 00D6
ZIF1 00DA  ZIF2 00DE  ZIF3 00E2  ZIF4 00E6  ZIF5 00EA  ZIF6 00EE  ZIF7 00F2  ZIF8 00F6
ZIF9 00FA  ZIFA 0067  ZIFB 0074

```

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.2.4 (Page 6)

Operation for input

1st Display selection

- Operate a push-button for selecting one of the figures (1 to 6) corresponding to the desired display.
- Operate push-button for column A or B.

2nd Figure input

- Input of the corresponding number (max. 4 digits).
- Operating of the Q-push-button (transfer to display).

3rd Display reset

- Reset is automatically realized by a new figure input or by
- operating the Q-push-button without figure input.

Components for circuit 10.2

		Ordering code
1	Microcomputer-IC	SAB 8748-8-D
1	I/O-expansion-IC	SAB 8243-D
12	Display modules	LCM 1001
12	AND-gate ICs	4081 BDC
2	4 to 16-decoder-ICs	4514 BF
1	Hex-buffer IC	4050 BDC
1	Monoflop-IC	4047 BDC
4	Diodes	BAY 61
1	Crystal, type A	5.990400 MHz
1	Voltage regulator	TDB 7805 T
1	Rectifier	B 1912-
		B 80 C 1500/1000
1	Transformer Tricoll	Type 45
2	Polypropylene-capacitors	22 pF/630 V
1	Polypropylene-capacitor	100 pF/630 V
2	Tantalum-capacitors	1 µF/40 V
1	Electrolytic capacitor	47 µF/10 V
1	Electrolytic capacitor	470 µF/16 V
4	Resistors or	10 kΩ/0.5 W
1	Resistor network ¹⁾	4 × 1 kΩ
5	Resistors or	100 kΩ/0.5 W
1	Resistor network ¹⁾	5 × 10 kΩ
		Commerzstahl München
		B33063-B6220-F
		B33063-B6101-F
		B45181-C4105-M
		B41313-A3476-T
		B41283-A4477-T
		B51261-Z4103-J1
		B92442-A0102-J304
		B51261-Z4104-J1
		B92442-A0103-J305

¹⁾ When resistor networks are used the resistance is reduced by a factor of 10. The dividing ratio remains 10:1.

10.3 Moving News Panel with LEDs

Output and display of texts including an important operator information are not only limited to devices of data processing systems but they are more and more applied in other fields of electronics, e.g. in industrial and consumer as well as control engineering. If data of different kinds (e.g. program results, error indications, decision criteria, test results, etc.) are displayed as moving news, they have a striking effect calling the operator's attention.

The text can easily be read when each character remains for 0.25 s on the display. A special advantage of a moving news panel being controlled by a microcomputer is in that the information can immediately be modified. The described circuit of **fig. 10.3.1** operates with SAB 8748. Its program memory capacity (EPROM) is 1K Byte and up to 900 characters can be stored. If the microcomputer is replaced by another one incorporating a different program, the information which is to be displayed is also exchanged.

The described circuit offers the advantage in requiring a minimum of components. The single-chip microcomputer SAB 8748 operates in conjunction with an alphanumeric 16-segment-LED-display DL 2416. It incorporates memory decoder and driver.

Hardware

The ASCII-coded data is transferred from the SAB 8748 to the display ICs via the bus port (DB0 to DB6) and via the $\overline{WR}$ -output (strobe). The information at pins P20 and P21 addresses the specific digits of the display-IC DL 2416.

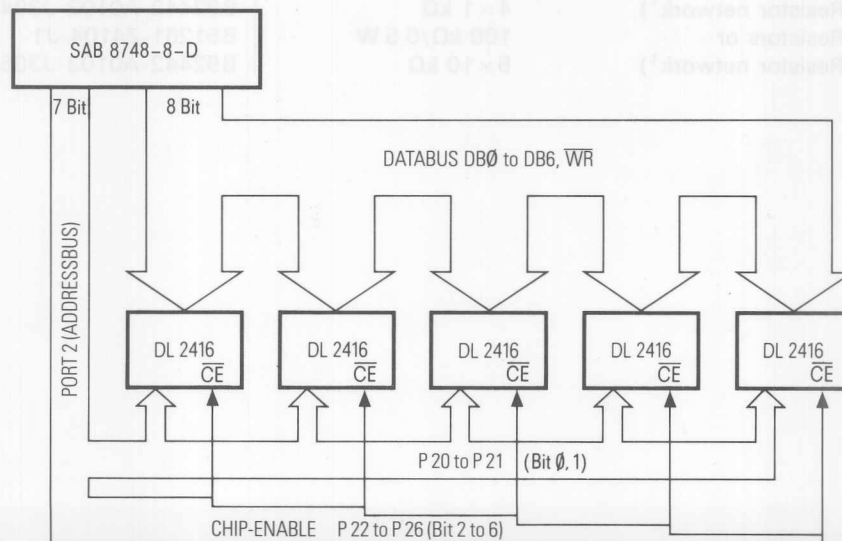


Fig. 10.3.1

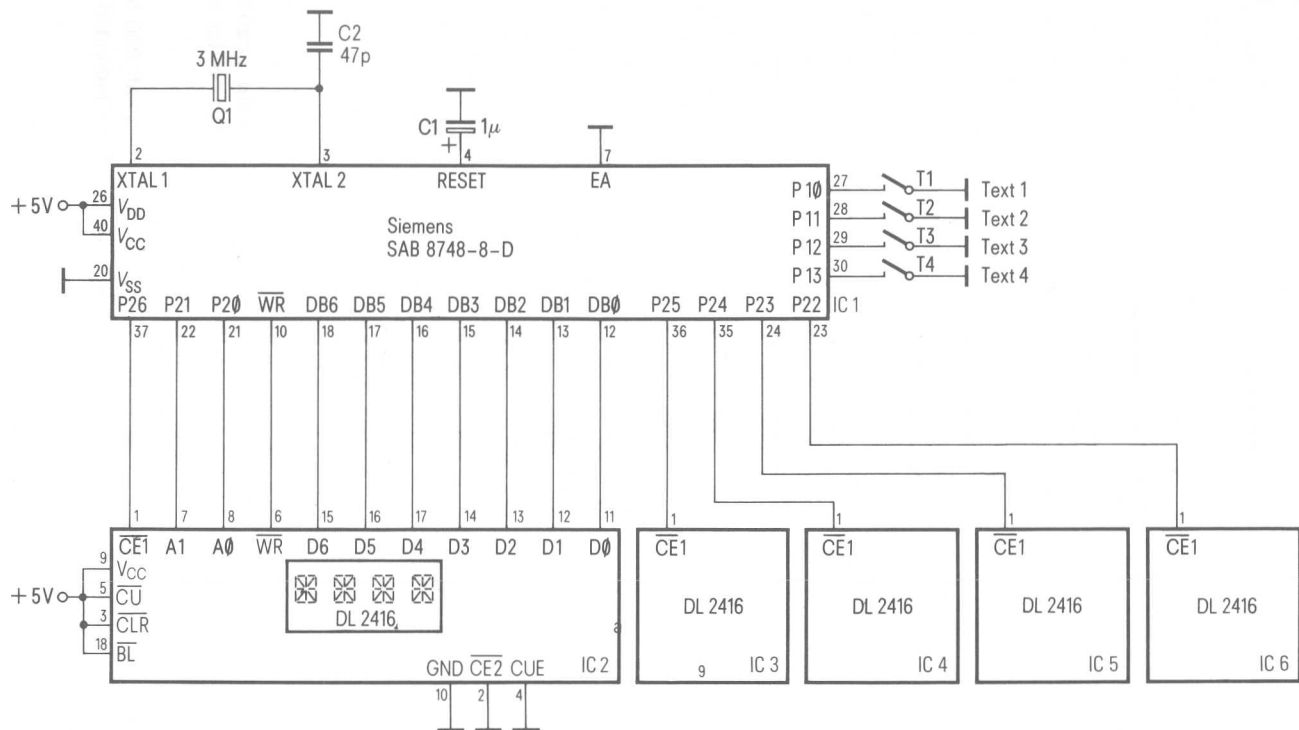


Fig. 10.3.2

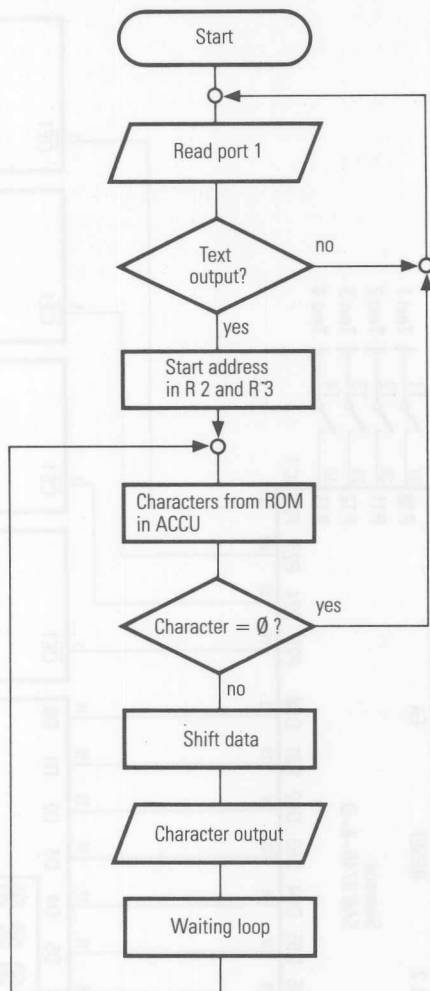


Fig. 10.3.3

The signals at P22 to P26 select the individual ICs via the chip enable input $\overline{CE1}$. When one pin of port 1 is connected to ground, the microcomputer supplies the corresponding text. An output of 4 different texts is possible.

The text may have any length as long as the memory capacity of 900 bytes is not exceeded. There are no additional components required than indicated in the circuit of **fig. 10.3.2**.

Software

The first 100 bytes of the EPROM are reserved for the program. As the program counter can only be read as data memory within 256 bytes, additional instructions are necessary (see listing). At the beginning of the program port 1 is read. If

a signal with low level is available at one of the pins, the starting address of the corresponding text is loaded to register 2 (low address) and 3 (high address). Now output registers 20H to 32H have to be filled with blanks. Then the first letter is transferred from text memory to data memory. Now the microprocessor operates in a waiting loop, determining the speed of the moving news. At an oscillator frequency of 3 MHz the timer has an overflow after $\frac{1}{3} \times 10^{-6} \mu s \times 15 \times 32 \times 256 = 40.96$ ms. The moving-news text is stepping four times per second after 6 overflows have occurred, that means the 900 characters need in total $3\frac{3}{4}$ minutes. If the 8-bit-word zero (figure 0, not the ASCII-character for 0) is read as character, the text end is recognized by the program. Therefore a counting is not necessary, that means all characters have been transferred. Now the program returns to read port 1.

The flowchart is shown in **fig. 10.3.3** and **fig. 10.3.4** presents the complete listing.

Components for circuit 10.3.2

			Ordering code
1	8-bit single-chip microcomputer (1-KByte-EPROM, 3-MHz-version)	SAB 8748-8-D	Q67120-C31-D88
5	4-digit alphanumeric LED- displays with memory, decoder and driver, (4 mm character height, 16 segments)	DL 2416	Q68000-A5577-F114
1	Crystal	3 MHz	—
4	Push buttons for pc board mounting, 2 break-make contacts, lateral operation		C42315-A60-A3

LOC	OBJ	LINE	SOURCE	STATEMENT
		1	%MACROFILE	PAGELLENGTH (100) PAGewidth (93)
		2	30.1.1980	
0000	0A	3	IN	A,P2 ;TASTENABFRAGE
0001	37	4	CPL	A
0002	120C	5	JB0	AUS1
0004	3212	6	JB1	AUS2
0006	5210	7	JB2	AUS3
0008	721E	8	JB3	AUS4
000A	0400	9	JMP	0
		10		
000C	BA80	11	AUS1:	MOV R2,#LOW (TEXT1 -1)
000E	BB00	12	MOV	R3,#HIGH (TEXT1-1) ;ADRESSE TEXT1
0010	0422	13	JMP	ANFANG
		14		
0012	BAA1	15	AUS2:	MOV R2,#LOW (TEXT2-1)
0014	BB00	16	MOV	R3,#HIGH (TEXT2-1) ;ADRESSE TEXT2
0016	0422	17	JMP	ANFANG
		18		
0018	BAC2	19	AUS3:	MOV R2,#LOW (TEXT3-1)
001A	BB00	20	MOV	R3,#HIGH (TEXT3-1) ;ADRESSE TEXT3
001C	0422	21	JMP	ANFANG
		22		
001E	BAE3	23	AUS4:	MOV R2,#LOW (TEXT4-1)
0020	BB00	24	MOV	R3,#HIGH (TEXT4-1) ;ADRESSE TEXT4
		25		
0022	55	26	ANFANG:	STRT T
0023	B020	27	MOV	R0,#20H
0025	BD14	28	MOV	R5,#20
0027	2320	29	MOV	A,#20H ;LEERSTELLE
0029	A0	30	LOECH:	MOV R0,A
002A	18	31	INC	R0
002B	ED29	32	DJNZ	R5,LOECH ;LEERSTELLE IN RAM 20H - 32H
002D	1464	33	SCHL:	CALL EINFUE ;NAECHSTES ZEICHEN
002F	C600	34	HALT:	JZ 0 ;LETZTES ZEICHEN ?
0031	BD14	35	MOV	R5,#20
0033	B020	36	MOV	R0,#20H
0035	20	37	SCHL1:	XCH A,R0 ;NACHSCHIEBEN
0036	18	38	INC	R0
0037	ED35	39	DJNZ	R5,SCHL1
0039	B020	40	MOV	R0,#20H
003B	BCF8	41	MOV	R4,#0F8H ;CHIP SELECT 1. DISPLAY
003D	1459	42	CALL	AUS4BY ;AUSGABE 4 STELLEN
003F	BCF4	43	MOV	R4,#0F4H ;CHIP SELECT 2. DISPLAY
0041	1459	44	CALL	AUS4BY
0043	BCEC	45	MOV	R4,#0ECH ;CHIP SELECT 3. DISPLAY
0045	1459	46	CALL	AUS4BY
0047	BCDC	47	MOV	R4,#10111000 ;CHIP SELECT 4. DISPLAY
0049	1459	48	CALL	AUS4BY
004B	BCBC	49	MOV	R4,#10111100 ;CHIP SELECT 5. DISPLAY
004D	1459	50	CALL	AUS4BY
004F	BD0A	51	MOV	R5,#10
0051	1655	52	WART:	JTF WEITER ;WARTESCHLEIFE 240 MS
0053	0451	53	JMP	WART:
0055	ED51	54	WEITER:	DJNZ R5,WART:
0057	042D	55	JMP	SCHL
		56		
		57	UNTER PROGRAMM	AUSGABE 4 STELLEN
		58	R0	POINTER ZUM AUSZUGEBENDEN ZEICHEN
		59	R4	CHIP SELECT UND 2 BIT ADRESSE
		60	R5	SCHLEIFENZAehler
		61		
0059	BD04	62	AUS4BY:	MOV R5,#4
005B	FC	63	AUS4B1:	MOV A,R4
005C	39	64	OUTL	P1,A
005D	1C	65	INC	R4
005E	F0	66	MOV	A,R0
005F	02	67	OUTL	BUS,A
0060	18	68	INC	R0
0061	ED5B	69	DJNZ	R5,AUS4B1
0063	83	70	RET	
		71	%EJECT	

Fig. 10.3.4 (Page 1)

LOC	OBJ	LINE	SOURCE STATEMENT
		72	;UNTERPROGRAMM EINHOELEN NAECHSTES ZEICHEN
		73	;ADRESSE IN R2 (LOW) UND R3 (HIGH)
		74	;SPRINGT AUF JEWEILIGEN SEITENANFANG
		75	;VOM DORT RETURN INS HAUPTPROGRAMM
		76	
0064	1A	77	EINFUE: INC R2
0065	FA	78	MOV A,R2
0066	966B	79	JNZ UNGEH
0068	8A02	80	MOV R2,#2
006A	1B	81	INC R3
006B	FB	82	UNGEH: MOV A,R3
006C	036F	83	ADD A,#JMPADR
006E	B3	84	JMPP 0A
006F	73	85	JMPADR: DB JMPADR +4
0070	76	86	DB JMPADR +7
0071	79	87	DB JMPADR +10
0072	7C	88	DB JMPADR +13
0073	FA	89	MOV A,R2
0074	047F	90	JMP DATEN ;PAGE 0 ANFANG DER DATEN
0076	FA	91	MOV A,R2
0077	2400	92	JMP 100H ;PAGE 1
0079	FA	93	MOV A,R2
007A	4400	94	JMP 200H ;PAGE 2
007C	FA	95	MOV A,R2
007D	6400	96	JMP 300H ;PAGE 3
		97	
007F	A3	98	DATEN: MOVP A,0A
0080	03	99	RET
0081	54455854	100	TEXT1: DB 'TEXTAUSGABE 1',0
0085	41555347		
0089	41424520		
008D	31202020		
0091	20202020		
0095	20202020		
0099	20202020		
009D	20202020		
00A1	00		
00A2	54455854	101	TEXT2: DB 'TEXTAUSGABE 2',0
00A6	41555347		
00AA	41424520		
00AE	32202020		
00B2	20202020		
00B6	20202020		
00BA	20202020		
00BE	20202020		
00C2	00		
00C3	54455854	102	TEXT3: DB 'TEXTAUSGABE 3',0
00C7	41555347		
00CB	41424520		
00CF	33202020		
00D3	20202020		
00D7	20202020		
00DB	20202020		
00DF	20202020		
00E3	00		
00E4	54455854	103	TEXT4: DB 'TEXTAUSGABE 4',0
00E8	41555347		
00EC	41424520		
00F0	34202020		
00F4	20202020		
00F8	20202020		
00FC	20202020		
0100	A3	104	MOVP A,0A ;DIESE BEFEHLE MUESSEN AN DEN
0101	03	105	RET ;STELLEN 100H 200H UND 300H
0102	20202020	106	DB ' ;STEHEN ,ANFANG JEDER "PAGE"
0106	00		
		107	END

USER SYMBOLS

ANFANG 0022	AUS1 000C	AUS2 0012	AUS3 0018	AUS4 001E	AUS4B1 005B
AUS4BY 0059	DATEN 007F	EINFUE 0064	HALT 002F	JMPADR 006F	LOECH 0029
SCHL 002D	SCHL1 0035	TEXT1 0081	TEXT2 00A2	TEXT3 00C3	TEXT4 00E4
UNGEG 006B	UARTE 0051	WEITER 0055			

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.3.4 (Page 2)

10.4 Time-Signal Controlled Clock with Microcomputer

The radio station DCF 77 transmitting a time signal is located near Frankfurt/Main. It operates with an extremely constant carrier frequency of 77.5 kHz and transmits the official atomic time scale of the Federal Physical Institute at Braunschweig (PTB=Physikalisch-Technische Bundesanstalt). The 27 kW-station covers a distance of approx. 800 km. Minute, hour, day of the week, day, month and year are available as BCD-coded signal. The seconds are transmitted in that the carrier is reduced by 25% of its amplitude.

The coded time-signal transmission starts after the 20th second of every minute and with every following second a bit is transmitted, that are 39 bits in total. The bit for the 59th second is suppressed in order to indicate the next minute. At a logical "0" the reduction lasts 0.1 s and at a "1" it is 0.2 s. The number of components required is a minimum. If there occurs a transmission interruption the clock operates independently with own reserve power. Program and circuit were developed with SAB 8748 the EPROM-version of microprocessor SAB 8048.

The clock comprises four modules: power supply, microcomputer with display driver, LED-display and receiver.

A constant supply voltage of 5 V is applied to the microcomputer (MC) and the preamplifier as shown in **fig. 10.4.1**. The displays have a supply voltage, which is controlled by a phototransistor as a sensor in that the brightness of the display depends on the ambient light.

The receiver circuit shown in **fig. 10.4.2** amplifies the front-end signal and demodulates it in that second-pulses with a length of 0.1 s or 0.2 s are generated. These pulses are supplied to the MC. The amplifier has three sections. It is built up with strong reference to RF-requirements.

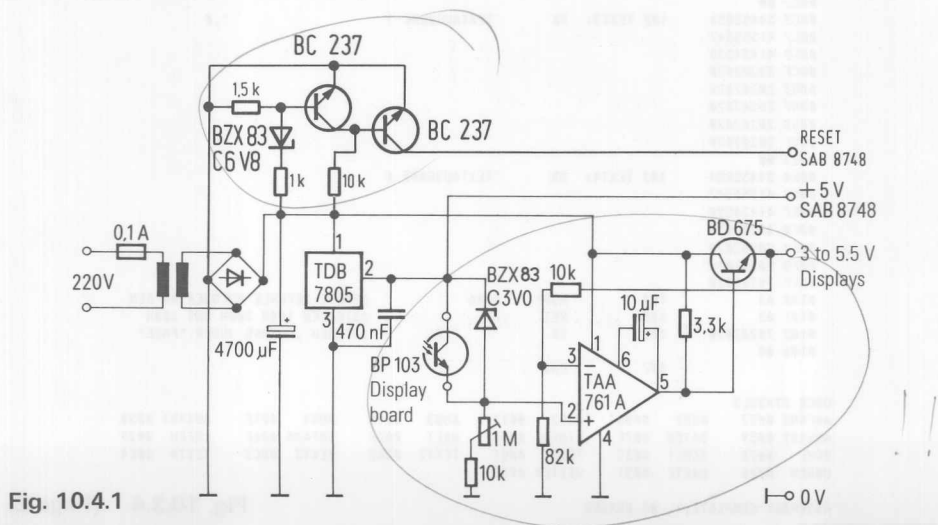
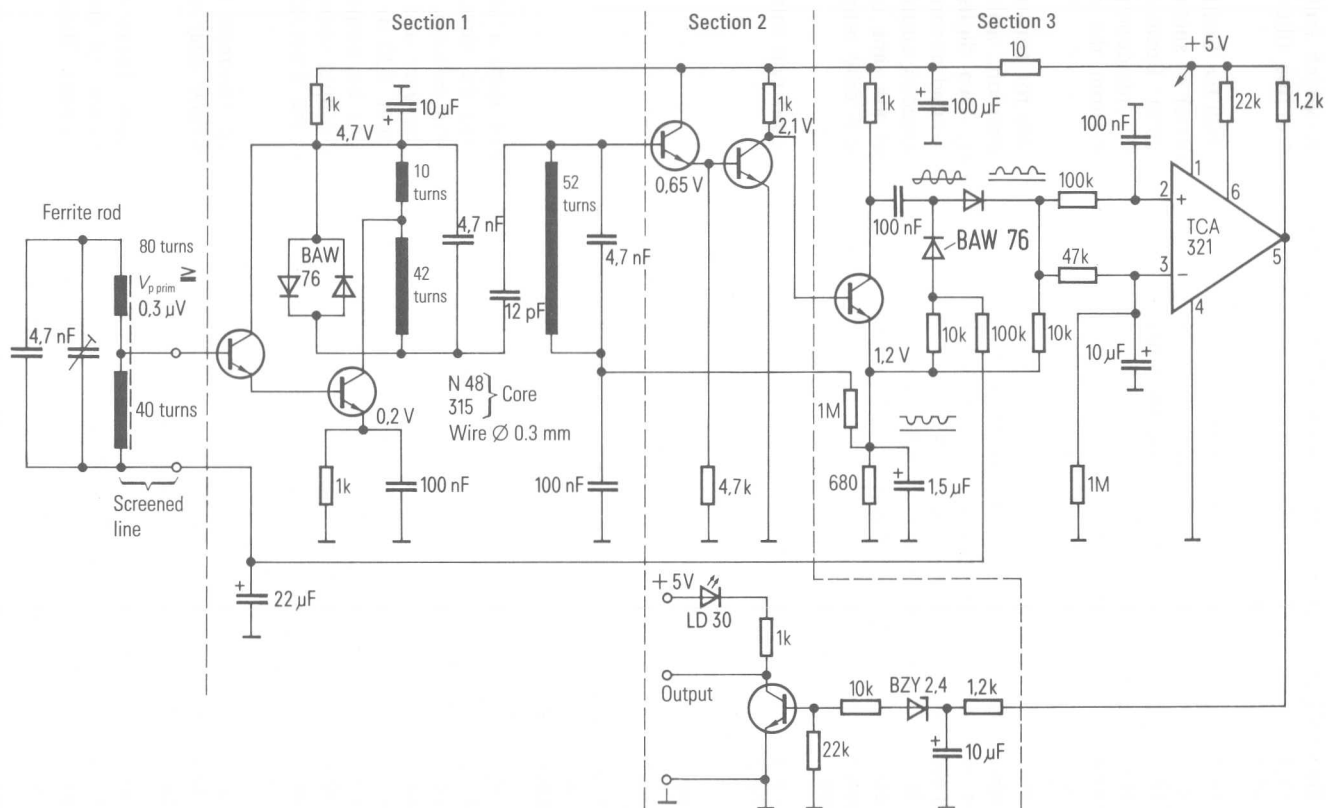


Fig. 10.4.1

Fig. 10.4.2.2



The signal of the ferrite rod coil is processed in the first section, which includes a Darlington stage and a band-pass filter. The secondary part of the filter has eventually to be screened by a shielding container.

This part of the total circuit determines the bandwidth of approx. 100 Hz. Section 2 amplifies the signal again and it is then supplied to the demodulator of section 3. The LED indicates a correct reception by flashing in a 1s-rhythm. Because of interference signals generated by the multiplex output stage of the microcomputer the ferrite aerial has to be placed in a distance of about 1 m from the clock circuit case and to be aligned to the transmitter.

The microcomputer shown in the circuit of **fig. 10.4.3** is responsible for converting the coded second-signals into a time-multiplex 7-segment information, which is applied to the LED-segments and anodes via driver transistors. Two digits are always supplied in parallel. At transmitter blackout the crystal-operated microcomputer is responsible for generating the time base and for continuous supplying the clock and calendar information. In case the transmission of the time signal is disturbed the decimal points (dp) of the display disappear and only reappear after the next correct transmission.

At a break down of the power supply the correct time is indicated two minutes after the supply voltage has reached again its specified value.

Program

The microcomputer is responsible for four tasks at the same time:

- read-in of the DCF 77-signals,
- display of clock time,
- continuous counting.

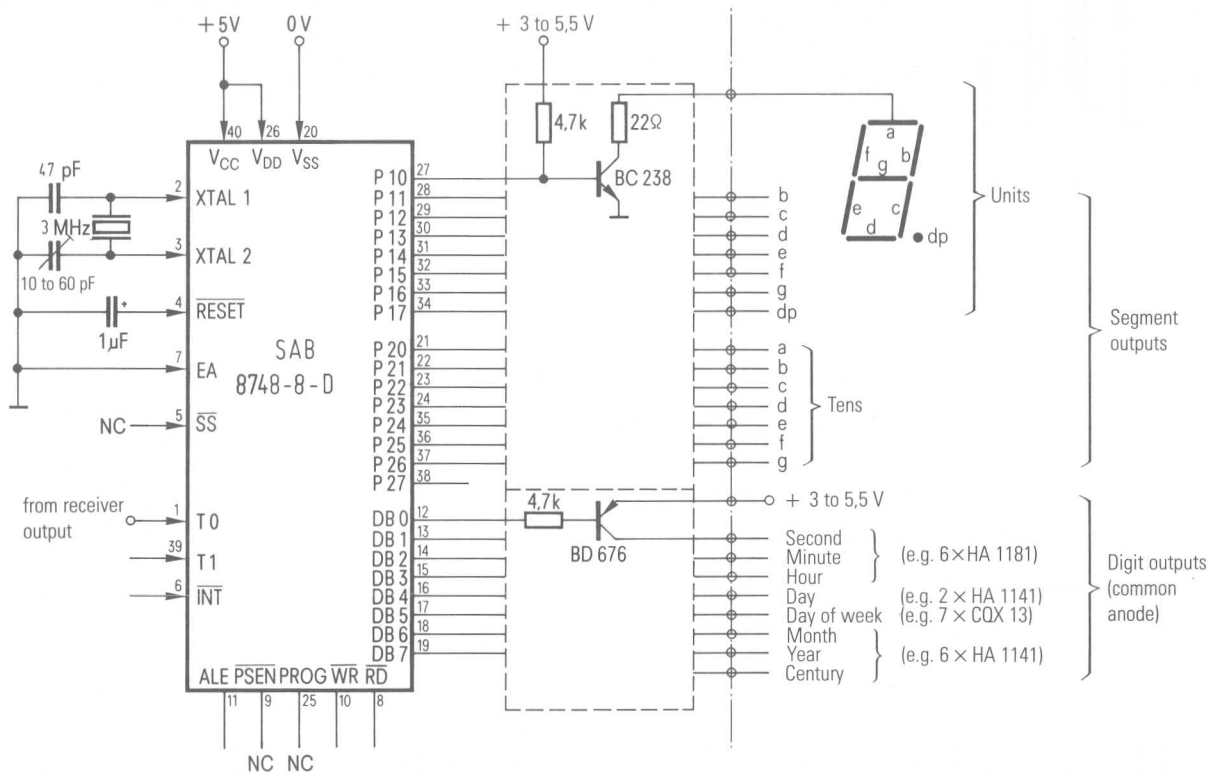
The read-in of the clock time is slowly obtained (second-pulses with a length of 100 ms or 200 ms) in that it can be interrupted for displaying the time. For the display 15 digits are read out, i.e. 2 digits for seconds, two for minutes, two for hours, two for the day, two for the month, four digits for the year and one for the day of the week. A multiplex frequency between 50 and 100 Hz and with a duty cycle between 5:1 and 10:1 should be realized. At an output of two 7-segment-decoded digits the duty cycle is 8:1. Therefore the output sequence minimum is $10 \text{ ms} : 8 = 1.25 \text{ ms}$. At a crystal frequency of 3 MHz the timer of the MC is incremented every $\frac{1}{3} \times 10^{-6} \times 15 \times 32 = 160 \text{ } \mu\text{s}$.

For the operational reserve of the clock at transmitter blackout 1s-steps have to be obtained ($1 \text{ s} : 160 \text{ } \mu\text{s} = 6250$ timer steps). At a timer overflow after every 10 steps an output sequence of $160 \text{ } \mu\text{s} \times 10 = 1.6 \text{ ms}$ is achieved.

There are $32 \times 20 = 640$ cycles at disposal between two overflows. These must be sufficient for output, operational reserve, alarm time recognition and, of course, for input. A second is reached after $1 \text{ s} : 1.6 \text{ ms} = 625$ output sequences. They can be separated into two loops of 25 sequences each.

Therefore the input program is interrupted every 1.6 ms. By the interrupt routine first the two digits are output then the alarm time is compared with the actual time and finally the clock continues to count.

Fig. 10.4.3



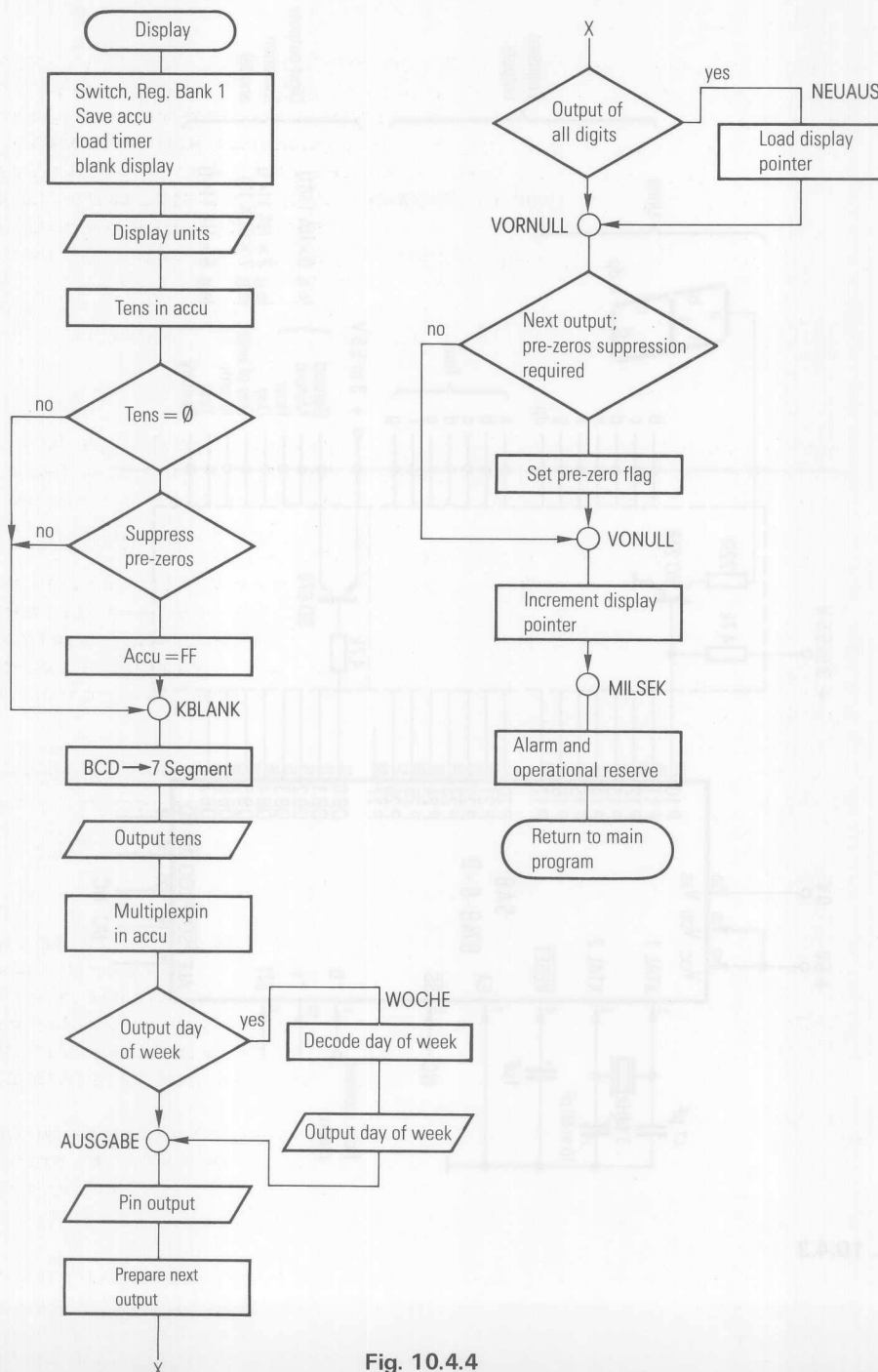


Fig. 10.4.4

Program part: display routine

Before the flowchart shown in **fig. 10.4.4** is established the memory capacity required for data has to be determined. Date and time need 8 bytes. They are stored in the RAM under addresses 20H to 27H. The access to the memory is achieved via register 0. Register 1 is used for addresses and reserve power function. Registers 2 and 3 serve as loop counters for seconds. Register 4 contains the information for the multiplexer output line. Register 5 stores the information as to whether the clock is running synchronously (0FFH) or not (07FH). Register 7 takes the accu content of the read routine. Flag 1 indicates the pre-zero suppression.

Fig. 10.4.5 shows the listing of the total program. The instructions are commented as far as necessary.

Alarm time

The device can be operated by a keyboard with 16 keys, connected to multiplex outputs and two further inputs (T_1 , INT). By this decimal keyboard alarm times can be set. The corresponding information is stored in an external non-volatile memory in that it is protected against power failure. For controlling other devices the date and time output can also be supplied in series or in parallel as BCD-coded information.

Table

Register listing at display routine
Output program for time-signal transmitter DCF 77
3 MHz- program

Register listing
Register bank 1

R0 Display pointer
R1
R2 1.6 ms-multiplexer, clock
R3 40 ms-multiplexer, clock
R4 Digit pin
R5 Decimal point
R6
R7 Accu

Data bytes

20 Output second
21 Output minute
22 Output hour
23 Output day
24 Output day of week
25 Output month
26 Output year
27 Output century

LOC	OBJ	LINE	SOURCE STATEMENT
1			;EMPFANGS PROGRAMM FUER ZEITZEICHENSENDER DCF 77
2			;3 MHZ PROGRAMM , KEINE WECKZEIT
3			;VIEHMANN WIS TE231 9.5.80
4			;REGISTER BELEGUNG
5			
6	R0		EINLESE POINTER
7	R1		
8	R2		40 MS FUER MINUTEN PULS
9	R3		SEKUNDEN BEIM EINLESEN
10	R4		SCHLEIFENZAELER
11	R5		1,6 MS EINLESEN
12	R6		40 MS "
13	R7		PARITY REGISTER
14			
15			;REGISTER BANK 1
16			
17	R0		ANZEIGE POINTER
18	R1		
19	R2		1,6 MS MULTIPLEXER ,UHR
20	R3		40 MS "
21	R4		DIGIT PIN
22	R5		DEZIMALPUNKT
23	R6		
24	R7		ACCU
25			
26			;DATEN BYTES
27			
28	20		AUSGABE SEKUNDE
29	21		" MINUTE
30	22		" STUNDE
31	23		" KALENDER TAG
32	24		" WOCHEN TAG
33	25		" MONAT
34	26		" JAHR
35	27		" JAHRHUNDERT
36	28		
37	29		EINLESE MINUTE
38	2A		" STUNDE
39	2B		" KALENDER TAG
40	2C		" WOCHEN TAG
41	2D		" MONAT
42	2E		" JAHR
43	2F		" JAHRHUNDERT
44			
45			\$EJECT

Fig. 10.4.5 (Page 1)

LOC	OBJ	LINE	SOURCE	STATEMENT
		46		
00F6		47	FREQUE EQU	246
		48		
		49		
0000 65		50	STOP	TCNT
0001 85		51	CLR	F0
0002 0409		52	JMP	RESET
0007		53	ORG	7
0007 2400		54	JMP	ANZEIG
0009 27		55	RESET: CLR	A
000A B820		56	MOV	R0,#20H
000C B908		57	MOV	R1,#8
000E A0		58	BLANK: MOV	0R0,A
000F 18		59	INC	R0
0010 E90E		60	DJNZ	R1,BLANK
0012 23F6		61	MOV	A,#FREQUE
0014 62		62	MOV	T,A
0015 D5		63	SEL	RB1
0016 BA19		64	MOV	R2,#25
0018 BB19		65	MOV	R3,#25
001A B820		66	MOV	R0,#20H
001C BC01		67	MOV	R4,#1
001E BD7F		68	MOV	R5,#7FH
0020 C5		69	SEL	R00
0021 2625		70	JNT0	EINS
0023 3623		71	WART0: JT0	WART0
0025 2625		72	EINS: JNT0	EINS
0027 55		73	STRT	T
0028 25		74	EN	TCNTI
0029 BA00		75	WART59: MOV	R2,#0
002B BD19		76	MOV	R5,#25
002D BE19		77	MOV	R6,#25
002F 362F		78	WARTMI: JT0	WARTMI
0031 2631		79	WART00: JNT0	WART00
0033 BD19		80	MOV	R5,#25
0035 BE19		81	MOV	R6,#25
0037 FA		82	MOV	A,R2
0038 03CF		83	ADD	A,#207
003A E686		84	JNC	FALSCH
003C 03FE		85	ADD	A,#254
003E F686		86	JC	FALSCH
0040 B800		87	MOV	R3,#0
0042 B65D		88	JF0	AUSFAL
0044 B81D		89	MOV	R0,#1DH
0046 B0FF		90	MOV	0R0,#0FFH
0048 B81A		91	MOV	R0,#1AH
004A B019		92	MOV	0R0,#25
004C 18		93	INC	R0
004D B019		94	MOV	0R0,#25
004F B820		95	MOV	R0,#20H
0051 B929		96	MOV	R1,#29H
0053 B000		97	MOV	0R0,#0
0055 BC07		98	MOV	R4,#7
0057 18		99	UEBERT: INC	R0
0058 F1		100	MOV	A,0R1

;SPRUNG NACH TIMER INTERRUPT ZUR ANZEIGEROUTINE
 ;BLANK IN ANZEIGE REGISTER 20 - 28 H
 ;TIMER LADEN MIT 256 - 10
 ;MILLISEKUNDENZAehler SETZEN
 ;ANZEIGE POINTER AUF SEKUNDEN
 ;DEZIMALPUNKT DUNKEL
 ;ENTSCHEIDEN OB 0 ODER 1 AN T0
 ;WARTEN AUF "0"
 ;WARTEN AUF 0 > 1 FLANKE
 ;STARTEN DER UHR
 ;1,6 MS EINLESE ZAEHLER SETZEN
 ;40MS " "
 ;WARTEN AUF "0"
 ;WARTEN AUF "0" -"1" FLANKE
 ;40 MS - ZAEHLER IN ACCU
 ;T < 1,96 SEK WARTEN AUF 59. SEKUNDE
 ;T > 2,04 SEK
 ;SEKUNDENZAehler ZURUECKSETZEN
 ;UEBERSPRINGEN,DA AUSFALL
 ;DEZIMALPUNKT RUECKSETZEN
 ;MILLISEKUNDENZAehler ZURUECKSETZEN
 ;POINTER ANZEIGE REGISTER
 ; " EINLESE REGISTER
 ;SEKUNDEN ANZEIGE RUECKSETZEN

Fig. 10.4.5 (Page 2)

LOC	OBJ	LINE	SOURCE	STATEMENT
0059	A0	101	MOV	R0, A ;UEBERTRAG VON EINLESE - IN
005A	19	102	INC	R1
005B	EC57	103	DJNZ	R4, UEBERT ;ANZEIGEREGISTER
005D	85	104	AUSFAL:	CLR F0
005E	BC07	105	MOV	R4, #7
0060	B830	106	MOV	R0, #30H
0062	C8	107	LOSCHE:	DEC R0
0063	B000	108	MOV	R0, #0
0065	EC62	109	DJNZ	R4, LOSCHE ;EINLESEREGISTER LOESCHEN
0067	14BE	110	SEK20:	CALL SEKUND ;0,1 S ODER 0,2 S
0069	FB	111	MOV	A, R3
006A	03EB	112	ADD	A, #235
006C	9667	113	JNZ	SEK20 ;21 SEKUNDEN NICHT VORBEI
006E	E6B6	114	JNC	FALSCH ; 0,1 S PULS
0070	BC08	115	MOV	R4, #0 ;SCHLEIFENZAehler FUER MINUTEN LADEN
0072	8F00	116	MOV	R7, #0 ;PARITY REGISTER LOESCHEN
0074	14E6	117	CALL	EINSCH ;MINUTEN EINSCHIEBEN
0076	537F	118	ANL	A, #7FH ;PARITY KILLEN
0078	14F4	119	CALL	ANSCH2
007A	12B6	120	JB0	FALSCH ;PARITAET UNGERADE
007C	BC07	121	MOV	R4, #7 ;SCHLEIFENZAehler STUNDEN LADEN
007E	14E6	122	CALL	EINSCH ;STUNDEN EINSCHIEBEN
0080	77	123	RR	A ;LEERSTELLE NACHSCHIEBEN
0081	533F	124	ANL	A, #3FH ;PARITY KILLEN
0083	14F4	125	CALL	ANSCH2
0085	12B6	126	JB0	FALSCH
0087	BC06	127	MOV	R4, #6 ;SCHLEIFENZAehler KALENDERTAG
0089	14E6	128	CALL	EINSCH
008B	BC02	129	MOV	R4, #2 ;2 MAL SCHIEBEN
008D	14F1	130	CALL	ANSCH1
008F	BC03	131	MOV	R4, #3 ;SCHLEIFENZAehler WOCHENTAG
0091	14E6	132	CALL	EINSCH
0093	BC05	133	MOV	R4, #5
0095	14F1	134	CALL	ANSCH1
0097	BC05	135	MOV	R4, #5 ;SCHLEIFENZAehler KALENDERMONAT
0099	14E6	136	CALL	EINSCH
009B	BC03	137	MOV	R4, #3
009D	14F1	138	CALL	ANSCH1
009F	BC08	139	MOV	R4, #8 ;SCHLEIFENZAehler KALENDERJAHR
00A1	14E6	140	CALL	EINSCH
00A3	18	141	INC	R0
00A4	0387	142	ADD	A, #087H
00A6	27	143	CLR	A
00A7	A7	144	CPL	C
00A8	1319	145	ADDC	A, #19H
00AA	57	146	DA	A
00AB	A0	147	MOV	R0, A ;19 ODER 20. JAHRHUNDERT
00AC	18	148	INC	R0
00AD	BC01	149	MOV	R4, #1
00AF	14E6	150	CALL	EINSCH ;PARITY BIT EINLESEN
00B1	FF	151	MOV	A, R7
00B2	12B6	152	JB0	FALSCH
00B4	0431	153	JMP	WART00 ;WARTEN AUF MINUTEN ANFANG
00B6	85	154	FALSCH:	CLR F0
00B7	95	155	CPL	F0 ;SETZEN FEHLER FLAG

Fig. 10.4.5 (Page 3)

LOC	OBJ	LINE	SOURCE	STATEMENT
00B8	B91D	156	MOV	R1, #1DH
00BA	B17F	157	MOV	R1, #7FH ;DEZIMALPUNKT SETZEN
00BC	0429	158	JMP	WART59 ;WARTEN AUF MINUTEN ANFANG
		159	%EJECT	

Fig. 10.4.5 (Page 4)

LOC	OBJ	LINE	SOURCE STATEMENT
		160	;UNTER PROGRAMM SEKUND
		161	;ERHOET R3 (SEKUNDEN ZAEHLER FUER EINLESE PROGRAMM)
		162	;SETZT BEI FEHLER F0
		163	;0 ODER 1 ALS INFORMATION IN CARRY
		164	
00BE	26BE	165	SEKUND: JNT0 SEKUND ;L > H FLANKE
00C0	BA00	166	MOV R2,00
00C2	BD19	167	MOV R5,025
00C4	BE19	168	MOV R6,025
00C6	36C6	169	SEKUN1: JT0 SEKUN1 ;H > L FLANKE
00C8	1B	170	INC R3 ;SEKUNDEN ERHOEHEN
00C9	FE	171	MOV A,R6 ;MILLISEKUNDEN IN ACCU
00CA	03E8	172	ADD A,0232
00CC	F6DF	173	JC FEHLER ;T < 0,08 SEK.
00CE	0305	174	ADD A,05
00D0	E6DF	175	JNC FEHLER ;T > 0,24 SEK.
00D2	FE	176	MOV A,R6 ;MILLISEK. IN ACCU
00D3	03E9	177	ADD A,0233
00D5	E6D9	178	JNC LOGI1 ;T > 0,12 SEK.
00D7	97	179	CLR C ;"0" IN CARRY
00D8	83	180	RET ;RUECKKEHR MIT "0" INS HAUPT PROGRAMM
00D9	37	181	LOGI1: CPL A
00DA	C6DF	182	JZ FEHLER ;0,12 SEK < T < 0,16 SEK.
00DC	97	183	CLR C
00DD	A7	184	CPL C ;"1" IN CARRY
00DE	83	185	RET ;RUECKKEHR MIT "1" INS HAUPT PROGRAMM
00DF	85	186	FEHLER: CLR F0
00E0	95	187	CPL F0 ;FEHLER FLAG SETZEN
00E1	B91D	188	MOV R1,01DH
00E3	B17F	189	MOV @R1,07FH ;DEZIMALPUNKT SETZEN
00E5	83	190	RET
		191	
		192	;EINSCHIEBE PROGRAMM
		193	;R0 POINTER ZUM EIN SCHIEBE BYTE
		194	;R4 SCHLEIFENZAehler
		195	;R7 PARITY REGISTER
		196	;RUFT UNTERPROGRAMM SEKUNDE AUF
		197	
00E6	14BE	198	EINSCH: CALL SEKUND ;0 ODER 1 IN CARRY
00E8	E6EB	199	JNC NERHOE
00EA	1F	200	INC R7
00EB	F0	201	NERHOE: MOV A,@R0 ;EINSCHIEBE BYTE IN ACCU
00EC	67	202	RRC A ;0 ODER 1 NACH SCHIEBEN
00ED	A0	203	MOV @R0,A ;EINSCHIEBE BYTE ZURUECK
00EE	ECE6	204	DJNZ R4,EINSCH
00F0	83	205	RET
		206	
		207	;UNTERPROGRAMM ANSCH
		208	;ERHOET R0 ALS EILESE POINTER
		209	;SCHIEBT @R0 UM R4 BITS NACH RECHTS
		210	;LAED PARITY REGISTER IN ACCU
		211	
00F1	77	212	ANSCH1: RR A
00F2	ECF1	213	DJNZ R4,ANSCH1
00F4	A0	214	ANSCH2: MOV @R0,A

Fig. 10.4.5 (Page 5)

LOC	OBJ	LINE	SOURCE STATEMENT
00F5	18	215	INC R0
00F6	FF	216	MOV A,R7
00F7	83	217	RET
0100		218	ORG 100H
		219	
		220	*EJECT

Fig. 10.4.5 (Page 6)

LOC	OBJ	LINE	SOURCE STATEMENT
		221	
		222	;INTERRUPT BEDDIENUNG
0100	D5	223	ANZEIG: SEL RB1 ;UMSCHALTEN AUF RB1
0101	AF	224	MOV R7,A ;ACCU RETTEN
0102	23F6	225	MOV A,#FREQUE
0104	62	226	MOV T,A ;TIMER NEU LADEN
0105	23FF	227	MOV A,#0FFH
0107	02	228	OUTL BUS,A ;ANZEIGE VERDUNKELN
0108	B5	229	CPL F1 ;VOR NULL UNTERDRUECKUNG
0109	F0	230	MOV A,0R0 ;NAECHSTE ANZEIGESTELLE IN ACCU
010A	530F	231	ANL A,#0FH ;EINERSTELLE
010C	E3	232	MOV P3 A,0A ;BCD > 7 SEGMENT
010D	5D	233	ANL A,R5 ;DEZIMALPUNKT FUER ANZEIGE
010E	39	234	OUTL P1,A ;AUSGABE AN P1
010F	F0	235	MOV A,0R0
0110	47	236	SWAP A
0111	530F	237	ANL A,#0FH ;ZEHNERSTELLE
0113	9618	238	JNZ KBLANK ;KEINE 0
0115	7618	239	JF1 KBLANK ;JAHRESZAHL
0117	37	240	CPL A ;A = FF
0118	E3	241	KBLANK: MOV P3 A,0A ;BCD > 7 SEG.
0119	3A	242	OUTL P2,A ;AUSGABE ZEHNER
011A	FC	243	MOV A,R4 ;DIGIT PIN
011B	922F	244	JB4 WOCH
011D	37	245	AUSGAB: CPL A ;WOCHENTAG IN ANZEIGE
011E	02	246	OUTL BUS,A ;DIGIT AUSGABE
011F	FC	247	MOV A,R4
0120	E7	248	RL A ;NAECHSTES DIGIT VORBEREITEN
0121	1237	249	JB0 NEUAUS ;ALLE DIGITS AUSGEBEN
0123	C637	250	JZ NEUAUS ;PIN VERLOREN
0125	AC	251	MOV R4,A ;RUECK SPEICHERN
0126	A5	252	VORNUL: CLR F1
0127	5353	253	ANL A,#010011B ;0 = VORNULLEN UNTERDRUECKUNG
0129	962C	254	JNZ JAHRZA ;NAECHSTE AUSGABE VORNULLEN UNTERDRUECKEN
012B	B5	255	CPL F1
012C	18	256	JAHRZA: INC R0 ;AUSGABE REG + 1
012D	243E	257	JMP MILSEK ;SPRUNG MILLISEKUNDEN ERHOEHEN
012F	F0	258	WOCH: MOV A,0R0 ;WOCHENTAG IN ACCU
0130	4310	259	ORL A,#10H ;SEL WOCHENTAG WANDLUNG
0132	E3	260	MOV P3 A,0A ;WOCHENTAG PIN IN ACCU
0133	3A	261	OUTL P2,A ;WOCHENTAG PIN AUSGEBEN
0134	FC	262	MOV A,R4
0135	241D	263	JMP AUSGAB ;ZURUECK ZUR AUSGABE
0137	B01F	264	NEUAUS: MOV R0,#1FH ;POINTER AUF SEKUNDEN
0139	BC01	265	MOV R4,#1
013B	B5	266	CPL F1
013C	2426	267	JMP VORNUL
013E	EAD1	268	MILSEK: DJNZ R2,RUECK ;40 MILSEK NICHT VORBEI
0140	BA19	269	MOV R2,#25
0142	EBD1	270	DJNZ R3,RUECK ;1 SEK
0144	BB19	271	MOV R3,#25
0146	B920	272	MOV R1,#20H
0148	F1	273	MOV A,0R1 ;SEKUNDEN IN ACCU
0149	0301	274	ADD A,#1
014B	57	275	DA A

Fig. 10.4.5 (Page 7)

LOC	OBJ	LINE	SOURCE STATEMENT	
014C	A1	276	MOV @R1,A	;SEK + 1 IN SEK REG.
014D	03A0	277	ADD A,#0A0H	
014F	E6D1	278	JNC RUECK	;60 SEK NOCH NICHT VORBEI
0151	27	279	CLR A	
0152	A1	280	MOV @R1,A	;0 IN SEK REG
0153	19	281	INC R1	
0154	F1	282	MOV A,@R1	;MIN IN ACCU
0155	0301	283	ADD A,#1	
0157	57	284	DA A	
0158	A1	285	MOV @R1,A	;MIN +1
0159	03A0	286	ADD A,#0A0H	
015B	E6D1	287	JNC RUECK	;60 MIN
015D	27	288	CLR A	
015E	A1	289	MOV @R1,A	;0 IN MINUTEN REG.
015F	19	290	INC R1	
0160	F1	291	MOV A,@R1	;STUNDEN IN ACCU
0161	0301	292	ADD A,#1	
0163	57	293	DA A	
0164	A1	294	MOV @R1,A	;H + 1 IN H REG
0165	03DC	295	ADD A,#0DCH	
0167	E6D1	296	JNC RUECK	;24 H
0169	B100	297	MOV @R1,#0	;0 IN STUNDEN
016B	19	298	INC R1	
016C	F1	299	MOV A,@R1	;TAG
016D	0301	300	ADD A,#1	
016F	57	301	DA A	
0170	A1	302	MOV @R1,A	
0171	19	303	INC R1	
0172	F1	304	MOV A,@R1	;WOCHENTAG
0173	17	305	INC A	
0174	A1	306	MOV @R1,A	
0175	72CD	307	JB3 MONTAG	;WOCHENANFANG
0177	C9	308	KEINON: DEC R1	
0178	F1	309	MOV A,@R1	;KALENDERTAG
0179	03D7	310	ADD A,#0D7H	
017B	E6D1	311	JNC RUECK	;28 TAGE NOCH NICHT VORBEI
017D	F1	312	MOV A,@R1	
017E	03CF	313	ADD A,#0CFH	
0180	F6AA	314	JC DREISI	;30 TAGE VORBEI
0182	B925	315	MOV R1,#25H	
0184	F1	316	MOV A,@R1	;MONAT
0185	03FE	317	ADD A,#0FEH	
0187	96D1	318	JNZ RUECK	;KEIN FEBRUAR
0189	19	319	INC R1	
018A	F1	320	MOV A,@R1	;JAHR
018B	5313	321	ANL A,#13H	
018D	C6A3	322	JZ SCHALT	;SCHALTJAHR
018F	F1	323	MOV A,@R1	
0190	531B	324	ANL A,#1BH	
0192	D312	325	XRL A,#12H	
0194	C6A3	326	JZ SCHALT	;SCHALTJAHR
0196	B923	327	MONAT: MOV R1,#23H	
0198	B101	328	MOV @R1,#1	;1 . KALENDERTAG
019A	B925	329	MOV R1,#25H	
019C	F1	330	MOV A,@R1	

Fig. 10.4.5 (Page 8)

LOC	OBJ	LINE	SOURCE STATEMENT
019D	0301	331	ADD A,#1
019F	57	332	DA A
01A0	A1	333	MOV @R1,A ;MONAT +1
01A1	24BD	334	JMP JAHR
01A3	B923	335	SCHALT: MOV R1,#23H
01A5	F1	336	MOV A,@R1 ;KALENDERTAG
01A6	12D1	337	JB0 RUECK ;29. FEB. SCHALTJAHR
01A8	2496	338	JMP MONAT
01AA	B923	339	DREISI: MOV R1,#23H
01AC	F1	340	MOV A,@R1 ;KALENDERTAG
01AD	3296	341	JB1 MONAT ;31. KALENDERTAG
01AF	B925	342	MOV R1,#25H
01B1	F1	343	MOV A,@R1 ;MONAT
01B2	72B9	344	JB3 AUGUST
01B4	92B9	345	JB4 AUGUST
01B6	37	346	CPL A
01B7	1296	347	JB0 MONAT ;APRIL, JUNI
01B9	1296	348	AUGUST: JB0 MONAT ;SEPT., NOV
01BB	24D1	349	JMP RUECK ;MONAT HAT 31 TAGE
01BD	D313	350	JAHR: XRL A,#13H
01BF	96D1	351	JNZ RUECK ;KEIN 1.1.
01C1	17	352	INC A
01C2	A1	353	MOV @R1,A ;JANUAR IN MONATS REG.
01C3	19	354	INC R1
01C4	61	355	ADD A,@R1 ;JAHR + 1
01C5	57	356	DA A
01C6	A1	357	MOV @R1,A
01C7	19	358	INC R1
01C8	27	359	CLR A
01C9	71	360	ADDC A,@R1 ;JAHRHUNDERT
01CA	A1	361	MOV @R1,A
01CB	24D1	362	JMP RUECK
01CD	B101	363	MONTAG: MOV @R1,#1 ;MONTAG IN WOCHENTAG REG
01CF	2477	364	JMP KEIMON
01D1	FF	365	RUECK: MOV A,R7 ;ACCU RUECKSPEICHERN
01D2	C5	366	SEL RB0
01D3	EDE5	367	DJNZ R5,RUECK1
01D5	BD19	368	MOV R5,#25
01D7	2A	369	XCH A,R2
01D8	0301	370	ADD A,#1
01DA	2A	371	XCH A,R2
01DB	E6E1	372	JNC DEC40H
01DD	D5	373	SEL RB1
01DE	BD7F	374	MOV R5,#7FH
01E0	C5	375	SEL RB0
01E1	EEE5	376	DEC40H: DJNZ R6,RUECK1
01E3	BE19	377	MOV R6,#25
01E5	93	378	RUECK1: RETR
		379	
		380	\$EJECT

Fig. 10.4.5 (Page 9)

LOC	OBJ	LINE	SOURCE STATEMENT
0300		381	ORG 300H
0300 BF		382	DB 0BFH ;0
0301 86		383	DB 086H ;1
0302 DB		384	DB 0DBH ;2
0303 CF		385	DB 0CFH ;3
0304 E6		386	DB 0E6H ;4
0305 ED		387	DB 0EDH ;5
0306 FD		388	DB 0FDH ;6
0307 87		389	DB 087H ;7
0308 FF		390	DB 0FFH ;8
0309 EF		391	DB 0EFH ;9
030F		392	ORG 30FH
030F 80		393	DB 80H ;BLANK
0310 80		394	DB 80H
0311 81		395	DB 81H ;WOCHENTAGE
0312 82		396	DB 82H
0313 84		397	DB 84H
0314 88		398	DB 88H
0315 90		399	DB 90H
0316 A0		400	DB 0A0H
0317 C0		401	DB 0C0H
		402	
03FF		403	ORG 3FFH
03FF 80		404	DB 80H
		405	END

USER SYMBOLS

ANSCH1 00F1	ANSCH2 00F4	ANZEIG 0100	AUGUST 01B9	AUSFAL 005D	AUSGAB 011D	BLANK 000E	DEC40M 01E1
DREISI 01AA	EINS 0025	EINSCH 00E6	FALSCH 00B6	FEHLER 00DF	FREQUE 00F6	JAHR 01BD	JAHRZA 012C
KBLANK 0118	KEIMON 0177	LOGI1 00D9	LOSCH 0062	MILSEK 013E	MONAT 0196	MONTAG 01CD	NERHOE 00EB
NEUAUS 0137	RESET 0009	RUECK 01D1	RUECK1 01E5	SCHALT 01A3	SEK20 0067	SEKUN1 00C6	SEKUND 00BE
UEBERT 0057	VORNUL 0126	WART00 0031	WART59 0029	WARTA0 0023	WARTMI 002F	WOCHE 012F	

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.4.5 (Page 10)

Components for circuit 10.4.1

		Ordering code
1 Operational amplifier	TAA 761 A	Q67000-A522
1 Positive voltage regulator	TDB 7805	Q67000-A1047
1 Phototransistor	BP 103 II	Q62702-P79-S1
2 Transistors	BC 237	Q62702-C697
1 Transistor	BD 675	Q62702-D238
1 Z-diode	BZX C3V0	Q62702-Z1064-F82
1 Z-diode	BZX C6V8	Q62702-Z1073-F82
1 Bridge rectifier	C 1406- B 40 C 3700/2200	C67067-A1786-A2
1 MKT-layer capacitor	470 nF/100 V	B32560-D1474-K
1 Electrolytic capacitor	10 μ F/25 V	B41313-A5106-T
1 Electrolytic capacitor	4700 μ F/10 V	B41010-C3478-T
1 Resistor	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	1.5 k Ω /0.5 W	B51261-Z4152-J1
1 Resistor	3.3 k Ω /0.5 W	B51261-Z4332-J1
3 Resistors	10 k Ω /0.5 W	B51261-Z4103-J1
1 Resistor	82 k Ω /0.5 W	B51261-Z4823-J1
1 Potentiometer	1 M Ω	—

Components for circuit 10.4.2

1 Operational amplifier	TCA 321	Q67000-A1006
4 Transistors	BC 414 C	Q62702-C376-V2
4 Diodes	BAW 76	Q62702-A397
1 LED	LD 30	Q62705-P23
1 Styroflex capacitor	12 pF/160 V	B31861-A1120-F
3 Styroflex capacitors	4.7 nF/160 V	B33063-B1472-H
3 MKT-layer capacitors	100 nF/100 V	B32560-D1104-K
1 Tantalum capacitor	1.5 μ F/25 V	B45181-C3155-M
3 Electrolytic capacitors	10 μ F/6.3 V	B41313-A2106-V
1 Electrolytic capacitor	22 μ F/10 V	B41313-A3226-T
1 Ferrite rod	104 $\times$ 0.25 mm	B61610-J
2 Pot cores with glued threaded sleeve	RM5/Nh8/Az315 nH	B65805-N0315-A048
1 Clamp		B65806-C2001-X000
1 Coil former, 6 pins, 2 sections		B65806-D1001-D002
1 Adjusting screw, green (material N22)		B65806-B3001-X022

Components for circuit 10.4.3

			Ordering code
1	Single-chip microcomputer	SAB 8048-8-D	Q67120-C31-D88
8	Transistors	BC 238	Q62702-C698
8	Transistors	BD 676	Q62702-D239
7	LEDs	CQX 13 I	Q62703-Q144-S1
8	LED-displays	HA 1141 r	Q68000-A3843
6	LED-displays	HA 1181 r	Q68000-A3878
1	Polypropylene capacitor	47 pF/630 V	B33063-B6470-F
1	Tantalum capacitor	1 μ F/40 V	B45181-B4105-M
1	Crystal	3 MHz	—
8	Resistors	22 Ω /0.5 W	B51261-Z4220-J1
10	Resistors	4.7 k Ω /0.5 W	B51261-Z4472-J1

10.5 Gray Scale Generator for TV Applications

The following design example is to demonstrate capability and universality of the one-chip-microcomputer SAB 8048. With this MC defined bit patterns can be generated at its ports by a special software program, that means a gray scale with 6 steps as well as line synchronizing pulses and picture repetition pulses with line interlacing are produced. This generating is mainly obtained by instructions which realize directly a logical AND-operation of the selected output port and a set mask. In this case the content of the accu is not influenced. By these instructions a defined setting and resetting of single bits is possible without changing the other bits of the port. Therefore a train of square-wave pulses, offering also a duty cycle of 2:1, can be generated. The pulse repetition period covers 4 MC-clock cycles. If a crystal with a frequency of 6 MHz is selected for operating the MC, square-wave pulses with a frequency of 100 kHz can be generated. In the described application a crystal frequency of 5.15625 MHz has been selected to produce pulses with a standardized width.

The circuit is shown in **fig. 10.5.1**. The three outputs P10 to P12 of the MC are connected to the address-inputs of an 8-channel-analog-multiplexer, type 4051. Eight potentiometers connected to the 4051 adjust synchronizing white and black level as well as the 5 gray half tones. The output signal of the analog-multiplexer is applied to the buffer transistor BF 254, which supplies at its output a composite signal with an amplitude of $1 V_{PP}$ (at 75Ω). A resistor matrix, controlled by 3 address bits, can also be used instead of analog-multiplexer and adjustment potentiometers. For test purposes the pulse of the first tail (TVB) is available at P 16 and at P 17 the pulse for the 10th tail.

Program

The listing of the complete program with 195 bytes is shown in **fig. 10.5.2**. The corresponding functions are commented.

After operating the RESET-push-button all outputs are set to zero.

The program jumps to line 191.

Before and after the line repetition pulses a half line is added at every second picture repetition to realize a line interlacing. Besides that the following subroutines are called:

- subroutine for generating N-blanking-lines,
- subroutine for vertical gray scale and again
- subroutine for generating N-blanking lines.

Register R5 is loaded with number N, in this case $N=11$ lines. The gray scale has 282 lines. As a register can only be loaded with a decimal number of up to 255 the following trick is applied. The repeated section of the program after the symbolic address SMU01R (line 146) is written twice and filled up with several

301



LOC	OBJ	LINE	SOURCE STATEMENT
		1	\$MACROFILE
		2	\$PAGELENGTH(100)
		3	\$MOEHN B AT FE 14.5.80
		4	;
		5	GRAUTREPPENGEGENERATOR
		6	;
		7	\$NOGEN
		8	;
0000	2300	9	RESET: MOV A,#0 ;
0002	39	10	OUTL P1,A ;
0003	0484	11	JMP MUST1 ;
		12	;
		13	;
		14	\$INCLUDE(UBIWE1.SRC)
		15	;
		16	INTERPROGRAMM ZUR ERZEUGUNG VON BILDWECHSELIMPULSEN
		17	;
0005	00	18	RTRAB2: NOP ;
0006	00	19	NOP ;
0007	00	20	NOP ;
0008	00	21	NOP ;
0009	27	22	CLR A ;
		23	;
000A	8901	24	TRABR2: ORL P1,#1 ;
000C	39	25	OUTL P1,A ;
000D	EA05	26	DJNZ R2,RTRAB2 ;
000F	93	27	RETR ;
0010	27	28	UBIWE1: CLR A ;
0011	8941	29	ORL P1,#65 ; 1. TRABANT MIT TVB
0013	39	30	OUTL P1,A ;
0014	00	31	NOP ;
0015	00	32	NOP ;
0016	00	33	NOP ;
0017	BA03	34	MOV R2,#3 ;
		35	;
0019	140A	36	CALL TRABR2 ; 2. BIS 4. TRABANT
		37	;
001B	27	38	CLR A ;
001C	00	39	NOP ;
001D	00	40	NOP ;
001E	8901	41	ORL P1,#1 ;
0020	39	42	OUTL P1,A ; 5. TRABANT
0021	00	43	NOP ;
0022	00	44	NOP ;
0023	00	45	NOP ;
0024	BA05	46	MOV R2,#5 ;
		47	;
0026	9938	48	HPTIR2: ANL P1,#56 ;
0028	8901	49	ORL P1,#1 ; 1. BIS 5. HAUPTIMPULS
002A	27	50	CLR A ;
002B	00	51	NOP ;
002C	00	52	NOP ;
002D	00	53	NOP ;
002E	00	54	NOP ;
002F	EA26	55	DJNZ R2,HPTIR2 ;
0031	9938	56	ANL P1,#56 ;
		57	;
0033	8901	58	ORL P1,#1 ; 6. TRABANT
0035	39	59	OUTL P1,A ;
0036	00	60	NOP ;
0037	00	61	NOP ;
0038	00	62	NOP ;
0039	BA03	63	MOV R2,#3 ;
		64	;
003B	140A	65	CALL TRABR2 ; 7. BIS 9. TRABANT
		66	;
003D	00	67	NOP ;
003E	00	68	NOP ;
003F	00	69	NOP ;
0040	8901	70	ORL P1,#129 ; 10. TRABANT UND TRIGGERSIGNAL TNB
0042	39	71	OUTL P1,A ;
0043	93	72	RETR ;
		73	;
		74	;
		75	\$EJECT

Fig. 10.5.2 (Page 1)

LOC	OBJ	LINE	SOURCE STATEMENT
		76	*INCLUDE(UNDURS.SRC)
		= 77	; UNTERPROGRAMM ZUR ERZEUGUNG VON N DUNKELZEILEN
		= 78	;
0044	FD	= 79	UNDURS: MOV A,R5 ; EINGABE N UEBER R5
0045	AA	= 80	MOV R2,A ;
0046	CA	= 81	DEC R2 ;
0047	00	= 82	NOP ;
0048	00	= 83	NOP ;
0049	00	= 84	NOP ;
004A	00	= 85	NOP ;
004B	00	= 86	RUECK: NOP ;
		= 87	REPT 6
		= 88	NOP
		= 89	ENDM
0052	8901	= 96	ORL P1,#1 ; ZEILENSYNCHRONZEICHEN
0054	99FE	= 97	ANL P1,#254 ;
		= 98	REPT 9
		= 99	NOP
		= 100	ENDM
005F	EA4B	= 110	DJNZ R2,RUECK ;
0061	93	= 111	RETR
		= 112	
		113	*EJECT

Fig. 10.5.2 (Page 2)

LOC	OBJ	LINE	SOURCE STATEMENT
		114	*INCLUDE(USMU01.SRC)
		= 115	
		= 116	; SCHWARZWEISSBILDMUSTER 01 VERTIKALE GRAUTREPPE
		= 117	;
		= 118	;14.5.00
		= 119	;
0062	00	= 120	USMU01: NOP ;
0063	00	= 121	NOP ;
0064	00	= 122	NOP ;
0065	8901	= 123	ORL P1,#1 ; VORZEILE
0067	99F8	= 124	ANL P1,#248 ;
		= 125	REPT 16 ;
		= 126	NOP ;
		= 127	ENDM ;
0079	BA8D	= 144	MOV R2,#141 ;
		= 145	
007B	8901	= 146	SMU01R: ORL P1,#1 ; ZEILEN MIT GRAUTREPPE
007D	99F8	= 147	ANL P1,#248 ;
007F	00	= 148	NOP ;
0080	00	= 149	NOP ;
0081	8903	= 150	ORL P1,#3 ; ADS 3
0083	99FA	= 151	ANL P1,#250 ; ADS 2
0085	8906	= 152	ORL P1,#6 ; ADS 6
0087	8907	= 153	ORL P1,#7 ; ADS 7
0089	99FD	= 154	ANL P1,#253 ; ADS 5
008B	99FC	= 155	ANL P1,#252 ; ADS 4
008D	99F8	= 156	ANL P1,#248 ; ADS 0 SCHWARZWERT
008F	00	= 157	NOP ;
0090	00	= 158	NOP ;
0091	8901	= 159	ORL P1,#1 ;
0093	99F8	= 160	ANL P1,#248 ;
0095	00	= 161	NOP ;
0096	00	= 162	NOP ;
0097	8903	= 163	ORL P1,#3 ; ADS 3
0099	99FA	= 164	ANL P1,#250 ; ADS 2
009B	8906	= 165	ORL P1,#6 ; ADS 6
009D	8907	= 166	ORL P1,#7 ; ADS 7
009F	99FD	= 167	ANL P1,#253 ; ADS 5
00A1	99FC	= 168	ANL P1,#252 ; ADS 4
00A3	99F8	= 169	ANL P1,#248 ; ADS 0 SCHWARZWERT
00A5	EA7B	= 170	DJNZ R2,SMU01R ;
00A7	8901	= 171	ORL P1,#1 ;
00A9	99F8	= 172	ANL P1,#248 ;
00AB	93	= 173	RETR ;
		= 174	
		175	*EJECT

Fig. 10.5.2 (Page 3)

```

LOC OBJ      LINE      SOURCE STATEMENT
              176 $INCLUDE(UHALBS.SRC)
              = 177
              = 178 ; UNTERPROGRAMM FUER HALBZEILE (ZEILENSPRUNG)
              = 179 ;
              = 180 ;
00AC 00        = 181 UHALBS: NOP          ;
00AD 00        = 182             NOP          ;
00AE 00        = 183             NOP          ;
00AF 0901      = 184             ORL   P1,#1    ;
00B1 99FE      = 185             ANL   P1,#254  ;
00B3 93        = 186             RETR         ;
              = 187 ;
              = 188 ;
              = 189 ;
              = 190 ;
00B4 8D0B      191 MUST1: MOV     RS,#11      ; GRAUTREPPE MIT ZEILENSPRUNG
00B6 1410      192 MUSTE1: CALL   UBIWE1      ;
00B8 1444      193             CALL   UNDUR5   ;
00BA 1462      194             CALL   USMU01   ;
00BC 1444      195             CALL   UNDUR5   ;
00BE 14AC      196             CALL   UHALBS   ;
00C0 00        197             NOP          ;
00C1 00        198             NOP          ;
00C2 1410      199             CALL   UBIWE1   ;
00C4 14AC      200             CALL   UHALBS   ;
00C6 1444      201             CALL   UNDUR5   ;
00C8 1462      202             CALL   USMU01   ;
00CA 1444      203             CALL   UNDUR5   ;
00CC 04B6      204             JMP     MUSTE1   ;
              205 ;
              206 ;
              207             END

USER SYMBOLS
HPTIR2 0026  MUST1 00B4  MUSTE1 00B6  RESET 0000  RTRAB2 0005  RUECK 004B  SMU01R 007B  TRABR2 000A
UBIWE1 0010  UHALBS 00AC  UNDUR5 0044  USMU01 0062

```

ASSEMBLY COMPLETE, NO ERRORS

Note: For translation of the German comments pls. see preceding text.

Fig. 10.5.2 (Page 4)

NOP-instructions for time compensation. Now the loop counter R2 is only loaded with half of the line number (141).

Expansion possibilities

As for the program a quarter of the available memory capacity is only required, other subroutines can be added. If a code switch is connected to port 2, different picture patterns and different TV-standards can be generated by selecting the appropriate software program.

Components for circuit 10.5.1

		Ordering code
1 Single-chip MC	SAB 8748-D	Q67120-C37-D88
1 8-channel-analog-multiplexer	4051BCD	67100-Y234
1 Transistor	BF 254	Q62702-F201
1 Polypropylene capacitor	18 pF/630 V	B33063-B6180-F
8 Electrolytic capacitors	4.7 μ F/40 V	B41313-A7475-T
1 Tantalum capacitor	4.7 μ F/40 V	B45181-C4475-M
1 Crystal	5.15625 MHz	—
2 Resistors	1 k Ω /0.5 W	B51261-Z4102-J1
1 Resistor	10 k Ω /0.5 W	B51261-Z4103-J1
8 Potentiometers	2 k Ω	—

Additional application examples for microcomputers of the 8048-family are described in sections 4.3, 4.6, 4.7 and 6.6 of this booklet.

11. Application Examples for Personal Computer PC 100

The personal computer PC 100 fills a gap between microcomputer systems and minicomputers. It is utilized in applications of measuring, testing and controlling. Because of its simple operation the PC 100 is an excellent learning device for programmers or people, who are engaged in microcomputers and in computers in general.

The intention of the following programming examples is to help both beginners of BASIC-language and experienced engineers.

User programs being developed in BASIC with PC 100 are fully compatible with future models of the Siemens personal computer family.

If the described programs are to be used, it is advantageous in storing them on a magnetic tape of a conventional cassette recorder. In this case instruction POKE 41993,64 has to be set before the recorder is operated. Then instruction SAVE has to be typed and the RETURN-key has to be operated. Thereafter the word OUT= is displayed.

Then the T-key is to be operated
and an F= is shown on the display,
now the name for the program can be input. The length of name has not to exceed 5 letters.

When the expression "T=" is displayed, the 1-key has to be operated and the cassette recorder has to be turned on. Only when the recorder is running, the RETURN-key is to be pushed. Now figures, indicating the block number of the stored data, are displayed on the right side. If an upward arrow is shown on the left side of display, the storing has been finished.

Loading of program from the cassette recorder to the PC 100 is realized by instruction LOAD. Of course, the RETURN-key has to be operated, too.

In this case an IN= is displayed,
then the T-key has to be operated.

After display of F=
the program name has to be input.

After display of T=
the 1-key has to be pushed.

In this case the RETURN-key can be immediately operated and the computer waits as long as the corresponding program is found on the tape.

11.1 Program for Calculating Resonant Circuits

After the program "Berechnung von Schwingkreisen" (=calculation of resonant circuits) has been typed in or transferred from the cassette recorder, it is started by RUN-instruction (see fig. 11.1). On the display the word "SCHWINGKREIS" (=resonant circuit) is shown and shortly thereafter "C=?, L=?, F=?" and an upward arrow. Now a value for C, L or F has to be input to calculate capacitance, inductance or frequency of the resonant circuit.

Assuming the resonant capacitance is to be calculated then the C-key has to be pushed and the RETURN-key has to be operated. Then the display shows "F IN HZ?". Now the resonant frequency in Hz has to be typed in, e.g. 1 MHz with 1 E 6. Thereafter the RETURN-key is operated. Now the computer asks "L IN UH?" and requires a value for the resonant inductance in μH . Assuming the number 100 is typed in and the RETURN-key is operated then the capacitance is calculated. The display shows "C=253.302967 PF".

For a new calculation the N-key is operated. In this case the first question is displayed as to whether a frequency, a capacitance or an inductance has to be calculated.

Typing-in and calculating of resonant inductance and frequency is correspondingly realized. For jumping-back to the monitor program the RETURN-key has only to be operated instead of typing-in a value for C, L or F.

LIST

```
1 REM**B AT PELKA
2 REM**15.1.80
3 REM**SCHUK
4 REM**PROGRAMM ZUR BERECHNUNG VON SCHWINGKREISEN**
10 PRINT "SCHWINGKREIS":GOSUB 200
20 INPUT " C=?,L=?,F=";A$
30 IF A$="C" THEN 270
40 IF A$="L" THEN 140
50 IF A$="F" THEN 80
60 PRINT"FALSCH EINGABE":GOSUB 200:GOTO 20
80 INPUT"C IN PF ";C
90 INPUT "L IN UH ";L
100 F=1E9/((2*3.1415926*SQR(C*L))
110 IF F>1E6 THEN F=F/1E6:PRINT "F=";F;"MHZ":GOTO 220
120 IF F>1E3 THEN F=F/1E3:PRINT "F=";F;"KHZ":GOTO 220
130 PRINT "F=";F;"HZ":GOTO 220
140 INPUT "C IN PF ";C
150 INPUT "F IN HZ ";F
160 L=1E15/((2*3.1415926*F)*2*C)
170 IF L<1E-4 THEN L=L*1E6:PRINT "L=";L;"MH":GOTO 220
180 IF L<1 THEN L=L*1E3:PRINT "L=";L;"UH":GOTO 220
190 PRINT "L=";L;"MH":GOTO 220
200 FOR I=1 TO 1000:NEXT
210 RETURN
220 GET F$
230 IF LEN(F$)=0 THEN 220
240 F=ASC(F$)
250 IF F=78 GOTO 20
260 GOTO 220
270 INPUT "F IN HZ ";F
280 INPUT "L IN UH ";L
290 C=1E12/((2*3.1415926*F)*2*L)
300 IF C<1E-3 THEN C=C*1E6:PRINT "C=";C;"PF":GOTO 220
310 IF C<1 THEN C=C*1E3:PRINT "C=";C;"NF":GOTO 220
320 PRINT "C=";C;"UF":GOTO 220
330 END
```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.1

11.2 Program for Calculating Cutoff-Frequency of RC-Circuits

The listing for the program "Berechnung von RC-Gliedern" (=calculation of RC-circuits) is shown in **fig. 11.2**. After it has been typed-in or transferred from a cassette recorder, the program is started by instruction RUN. The display shows "GRENZFREQUENZ VON RC-GLIEDERN" (=cutoff frequency of RC-circuits) and shortly thereafter "R=?, C=?, FG=?" and an upward arrow.

Now a value for R, C or FG has to be typed-in for calculating resistance, capacitance or cutoff frequency of the RC-circuit.

Assuming the resistance is to be calculated the R-key has to be operated and then the RETURN-key has to be pushed. Now "C IN FARAD?" is displayed and the value for C in Farad has to be typed in, e.g. 100 μ F with 100E-6. Thereafter the PC 100 asks "FG IN HZ?" and requires the input for frequency. Assuming a number of 50 is typed in for the frequency and the RETURN-key is operated then the resistance is calculated. The display indicates "R=31.8309142 OHM".

For a new calculation the N-key is to be operated. In this case the first question is displayed as to whether the resistance, the capacitance or the cutoff-frequency is to be calculated.

Typing-in and calculating of capacitance and cutoff frequency for the RC-circuit is correspondingly realized. For jumping-back to the monitor program the RETURN-key has only to be operated instead of typing in R, C or FG.

```
LIST
1 REM**B AT PELKA
2 REM**20.5.80
3 REM**RC-GL
4 REM**PROGRAMM ZUR BERECHNUNG VON RC-GLIEDERN
10 PRINT"GRENZFREQUENZ VON":GOSUB 200
20 PRINT"RC-GLIEDERN":GOSUB 200
30 DIM A$(10)
40 INPUT"R=?,C=?,FG=";A$
50 IF A$="R"THEN160
60 IF A$="C"THEN 120
70 IF A$="FG"GOTO 80
75 PRINT "FALSCH EINGABE":GOSUB 200:GOTO 40
80 INPUT " R IN OHM ";R
90 INPUT "C IN FARAD ";C
100 F=1/(2*3.1416*R*C)
105 IF F>1E6 THEN F=F/1E6:PRINT"FG=";F;"MHZ":GOTO 220
110 IF F>1E3 THEN F=F/1E3:PRINT"FG=";F;"KHZ":GOTO 220
115 PRINT"FG=";F;"HZ":GOTO 220
120 INPUT " R IN OHM ";R
130 INPUT " FG IN HZ ";F
140 C=1E6/(2*3.1416*R*F)
145 IF C<1E-3 THEN C=C*1E6:PRINT"C=";C;"PF":GOTO 220
150 IF C<1 THEN C=C*1E3:PRINT"C=";C;"NF":GOTO 220
155 PRINT "C=";C;"UF":GOTO 220
160 INPUT " C IN FARAD ";C
170 INPUT " FG IN HZ ";F
180 R=1/(2*3.1416*C*F)
185 IF R>1E6 THEN R=R/1E6:PRINT"R=";R;"MOHM":GOTO 220
190 IF R>1E3 THEN R=R/1E3:PRINT"R=";R;"KOHM":GOTO 220
195 PRINT "R=";R;"OHM":GOTO 220
200 FOR I=1 TO 1000:NEXT
210 RETURN
220 GET F$
225 IF LEN(F$)=0 GOTO 220
230 F=ASC(F$)
240 IF F=78 GOTO 40
250 GOTO 220
260 END
```

Fig. 11.2

Note: For translation of the comments in German language pls. see preceding text.

11.3 Program for Converting Decimal Numbers to Hexadecimal Ones

Applications of microcomputers very often require a conversion from decimal numbers to hexadecimal ones or vice versa. This requirement can also be met by the PC100, if an additional ROM is used. But the decimal-to-hexadecimal conversion can also be realized by software as demonstrated by the following program. The length maximum is 20 bit for each number.

The listing is shown in **fig. 11.3**. After the program "Umwandlung einer Dezimalzahl" (=conversion of a decimal number) has been typed in or transferred from a cassette recorder, it is started by RUN-instruction. The display shows the word "DEZIMAL-ZAHL" (=decimal number) and an upward arrow.

The computer requires the input of a number which is less than 1048575 and the operation of the RETURN-key. Assuming the decimal number 64560 is typed in and the RETURN-key is pushed, the display indicates "HEXZAHL=0FC30H" (=hexadecimal number).

The input of a new number is possible by operating the N-key.

For jumping-back to the monitor program the RETURN-key has to be operated instead of typing-in a decimal number.

```
LIST
1 REM**B AT PELKA
2 REM**10.1.80
3 REM**DEZHE
4 REM**PROGRAMM ZUR UMWANDLUNG EINER DEZIMALZAHL
5 REM**IN EINE HEXZAHL(SEDEZIMALZAHL)
10 FOR N=1 TO 5
20 B(N)=16*(5-N)
30 NEXT N
40 INPUT " DEZIMALZAHL ";A
50 IF A<0 THEN PRINT " ZAHL IST NEGATIV":GOSUB 200
60 IF A>1048575 THEN PRINT "ZAHL IST > 20 BIT":GOSUB 200
80 B$=""
90 FOR N=1 TO 5
100 X=INT(A/B(N))
110 GOSUB 160
120 B$=B$+X$
130 A=A-X*B(N)
140 NEXT N
145 IF LEFT$(B$,2)=""00"THEN B$=RIGHT$(B$,LEN(B$)-1):GOTO 145
150 PRINT "HEXZAHL=";B$;"H"
155 GOTO 220
160 IF X<10 THEN X$=RIGHT$(STR$(X),1):RETURN
170 X$=CHR$(X+55)
180 RETURN
200 FOR I=1 TO 1000:NEXT
210 GOTO 40
220 GET F$
230 IF LEN(F$)=0 THEN GOTO 220
240 F=ASC(F$)
250 IF F=78 GOTO 40
260 GOTO 220
270 END
```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.3

11.4 Program for Converting Hexadecimal Numbers to Decimal ones

Very often a hexadecimal-to-decimal conversion is required. For this application the PC 100 can also be utilized, if an additional ROM is used. But the conversion can be realized by software, too. The following program "Umwandlung einer Hexzahl" (=conversion of a hexadecimal number) converts a hexadecimal number to a decimal one. The former is only limited by the feature of the PC 100 in that the highest representation number is $1.70141183 \times 10^{38}$.

The listing is shown in **fig. 11.4**. After the program has been typed-in or transferred from a cassette recorder, it is started by the RUN-instruction. The display shows the word "HEXZAHL" (=hexadecimal number) and an upward arrow. Now a hexadecimal number has to be typed-in as well as the H-key. Thereafter the RETURN-key has to be operated. If the H-key is not operated, another question "HEXZAHL?" is displayed. The new number can immediately be typed-in. It is insignificant as to whether leading zeros are input or not. If a wrong number has been typed in, the input status can be realized again by pushing the keys for X, for RETURN and then for N.

Assuming the hexadecimal number 0FE8DH is loaded and the RETURN-key is operated then the display indicates "DEZIMALZAHL=65165" (=decimal number).

```

LIST
1 REM**B AT PELKA
2 REM**14.1.88
3 REM**HEXDE
4 REM**PROGRAMM ZUR UMWANDLUNG EINER HEXZAHL
5 REM** (SEDEZIMALZAHL) IN EINE DEZIMALZAHL
10 INPUT "HEXZAHL ";A$
20 IF RIGHT$(A$,1)="X" THEN GOTO 220
30 IF RIGHT$(A$,1)="H" THEN GOTO 55
40 PRINT "MIT 'H' BEENDEN!"
50 GOTO 218
55 E=0:E1=LEN(A$)-1
60 FOR N=1 TO E1
70 C$=MID$(A$,N,1)
80 GOSUB 200
90 E=E+C*16^(E1-N)
100 NEXT N
180 PRINT "DEZIMALZAHL=";E
190 GOTO 220
200 C1=ASC(C$)
201 IF C1<48 THEN 217
202 IF C1>57 THEN 204
203 C=C1-48:RETURN
204 IF C1<64 THEN 217
205 IF C1>70 THEN 217
206 C=C1-55:RETURN
217 PRINT " FALSCH EINGABE"
218 FOR I=1 TO 1000:NEXT
219 GOTO 10
220 GET F$
230 IF LEN(F$)=0 THEN GOTO 220
240 F=ASC(F$)
250 IF F=78 GOTO 10
260 GOTO 220
270 END

```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.4

If the converted number is greater than 999999, then only the figurers are displayed due to the display function of the PC 100.

The input of a new number is possible by operating the N-key. In this case the display again indicates the question 'HEXZAHL?'.

For jumping-back to the monitor program the RETURN-key has to be operated instead of typing-in a hexadecimal number.

11.5 Output Program for ASCII-Equivalent of Keys Being Operated

For programming in BASIC-language it is very often important to know the ASCII-equivalents of keys being operated. There is a list in the BASIC-manual for all visible characters. However, less known is the fact that for control characters the decimal equivalent 0 to 26 can be loaded by simultaneous operating of CTRL-key and the key for one of letters A to Z.

With the following program "Ausgabe des ASCII-Aequivalents einer gedrückten Taste" the ASCII-equivalent of each key being operated can unconventionally and fast be indicated by operating the keys for "SHIFT" and "CTRL".

The listing is shown in **fig. 11.5**. After the program has been typed in or transfered from a cassette recorder, it is started by the RUN-instruction. The display shows the expression "TASTE DRUECKEN!" (= push key). After one of the keys is operated, the ASCII-equivalent is displayed, e.g. when the A-key is pushed, the display indicates "A=DEZIMAL-AEQUIVALENT 65" (=decimal equivalent).

For an invisible character, e.g. for CTRL C, the expression "=DEZIMAL-AEQUIVALENT 3" is shown.

For jumping-back the F₁-key has to be operated.

```
LIST
1 REM**B AT PELKA
2 REM**20.5.80
3 REM**ASCII
4 REM**PROGRAMM ZUR AUSGABE DES
5 REM**ASCII-AEQUIVALENTES EINER GEDRUECKTEN TASTE
6 PRINT"TASTE DRUECKEN !"
10 GET A$
15 IF LEN(A$)=0 THEN 10
20 A=ASC(A$)
30 PRINT A$;"=DEZ.AEQ.";A
40 GOTO 10
```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.5

11.6 Program for Initializing Serial Output

Pin "U" of the connector for external application is specified as a serial output "TTY PTR". It is an open-collector output of a NAND-gate. The peripheral device connected to the PC 100 has probably to be operated by an interface circuit that can be realized by an opto coupler and a current-limiting resistor connected to the +5 V-supply-line. The serial output is initialized by the program described in the following.

The listing is shown in **fig. 11.6**. Before the program "Initialisierung der seriellen Ausgabe am PC 100" (=initializing the serial output of PC 100) is typed in or transfered from a cassette recorder, the question "MEMORY SIZE" has to be answered by loading the number 4064 or a lower value, as the upper bytes of the memory are reserved for the output program.

This program is placed at very high byte numbers to keep sufficient space for other programs. It has to be considered that under no circumstances this program is erased by a NEW-instruction.

The serial interface is initialized by instruction 'RUN 59000'. First the question "BAUDRATE?" is shown on the display. In this case the following baud rates can be loaded: 110, 150, 300, 600, 1200, 2400, 4800 and 9600. After input of the baud rate the RETURN-key has to be operated. Thus the serial interface is initialized, that means all information shown on the PC 100-display is also available for the serial interface.

If programs are to be loaded on or transfered from a cassette recorder, the serial interface has to be turned off. This is realized by instruction "RUN 59300".

LIST

```

59000 REM**B AT FE KNOEPFLE
59001 REM**21.5.80
59002 REM**S.AUS
59003 REM**PROGRAMM ZUR INITIALISIERUNG DER
59004 REM**SERIELLEN AUSGABE AM PC100
59010 INPUT"BAUDRATE ?";B
59020 RESTORE
59030 READ A
59040 IF A<0 GOTO 59120
59050 IF A=B GOTO 59090
59060 READ A
59070 READ A
59080 GOTO 59030
59090 READ A:POKE 42007,A
59100 READ A:POKE 42008,A
59110 GOTO 59030
59120 POKE 41990,224
59130 POKE 41991,15
59140 READ A
59150 READ B
59160 IF B<0 THEN 59200
59170 POKE A,B
59180 A=A+1
59190 GOTO 59150
59200 POKE 4,224
59210 POKE 5,15
59220 X=USR(X)
59230 DATA 110,35,63,150,25,183,300,12,194,600,6,63
59240 DATA 1200,2,253,2400,1,93,4800,0,141,9600,0,37,-1
59250 DATA 4064,141,255,15,41,127,201,13,240,3,76,168,238
59260 DATA 169,10,32,168,238,173,255,15,76,168,238,-1
59270 END
59290 REM**AUSGABE ABSCHALTEN
59300 POKE41990,5:POKE41991,239
59310 END

```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.6

11.7 Program for Reading BCD-Data with 4.5 Digits

For external applications the PC 100 offers a connector, the pins of which can directly be applied with measuring data as shown in **fig. 11.7.1**. The data is suitably supplied as BCD-coded information. The maximum number that can be accepted is 19999. Positive values are only considered, as a polarity sign is not provided for. The data is read during the positive slope of the signal applied to pin CA₁ (20). The computer assigns the data to a nominal value with a tolerance range that has to be defined and loaded at the beginning. On the display the forming also informs of the value being measured:

display on the left side → too low,
display in the middle → measured value in the tolerance range,
display on the right side → too high.

When the N-key is operated, the following data is printed:

- total number of all measured and processed values,
- cumulative average of measured values,
- number of measured values being lower, within and higher than the tolerance range.

When the printing has been finished, the PC 100 continues to read the supplied data.

It is very important that all lines have defined levels and that they are not operated without loads. At output TTY-KYBD the base of the transistor being part of the PC 100 has to be protected by a 1 k Ω -series-resistor.

Program

The flowchart is demonstrated in **fig. 11.7.2** and **fig. 11.7.3** shows the program listing "Einlesen von BCD-Daten" (=input of BCD-data). Lines 25 to 40 are

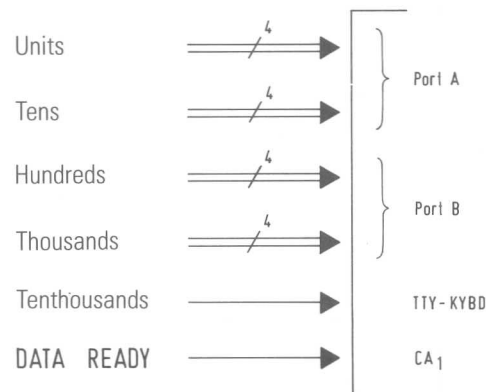


Fig. 11.7.1

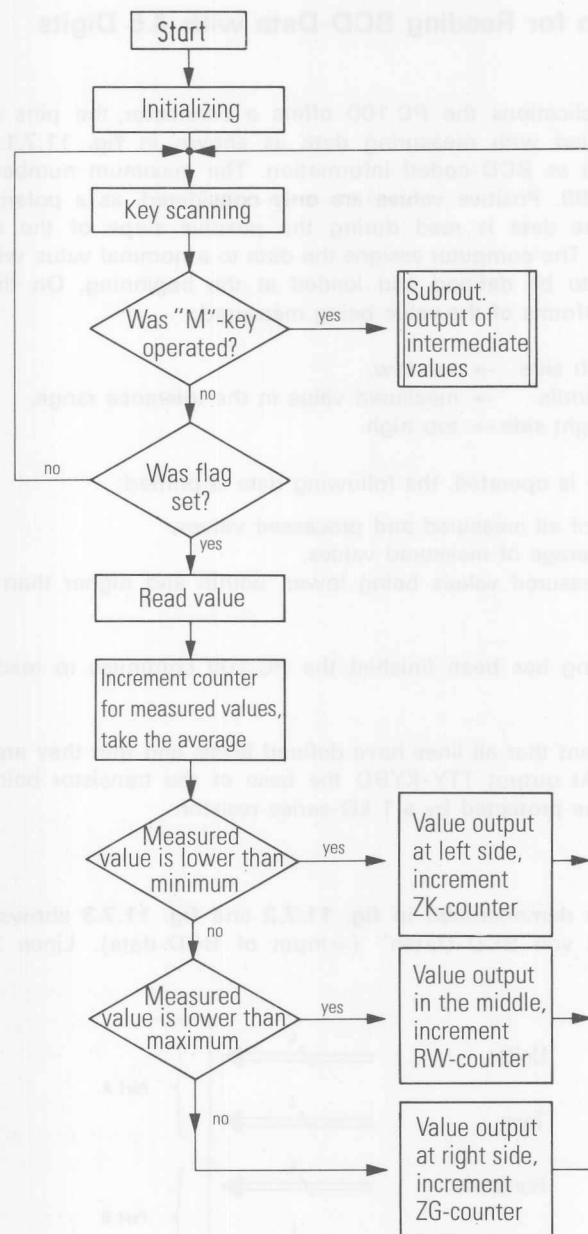


Fig. 11.7.2

LIST

```

1 REM**RS EBG V 3 BUETTNER
2 REM**22.5.80
3 REM**BCD
4 REM**PROGRAMM ZUM EINLESEN VON BCD-DATEN
5 POKE42001,0:REM ** DRUCKER AUS **
10 POKE40962,0:REM ** PORT B INPUT **
15 POKE40963,0:REM ** PORT A INPUT **
20 POKE40972,1:REM ** CA1 SETZT FLAG (ADR = 40973) **
21 REM ** BEI POSITIVER FLANKE **
25 INPUT"NENNWERT=";NW
30 INPUT"+ TOLERANZ IN % =" ;PT
40 INPUT"- TOLERANZ IN % =" ;MT
50 G1=NW-(NW*(MT*.01))
60 G2=NW+(NW*(PT*.01))
70 DEFFNB(X)=(BAND240)/16*1000+(BAND15)*100
80 DEFFNA(X)=(AAND240)/16*10+(AAND15)
85 DEFFNC(X)=(CAND64)/64*10000
90 GETA$:IFA$="H"THEN1000
100 IFPEEK(40973)AND2=2THEN120
110 GOTO90
120 A=PEEK(40961):B=PEEK(40960):C=PEEK(43008)
130 Z=FNA(X)+FNB(X)+FNC(X):Y=Y+Z:I=I+1:D=INT(Y/I+.5)
140 IFZ<G1THEN100
150 IFZ<G2THEN200
160 PRINTTAB(13);Z:ZG=ZG+1
170 GOTO90
180 PRINTZ:ZK=ZK+1
190 GOTO90
200 PRINTTAB(8);Z:RW=RW+1
210 GOTO90
1000 PRINTSPC(40);"GESANTANZAHL ";I
1010 PRINT"MITTELWERT: ";D
1020 PRINT"INNERHALB TOL.: ";RW
1030 PRINT"ZU KLEIN: ";ZK
1040 PRINT"ZU GROSS: ";ZG
1050 PRINT"*****"
1060 PRINT" "
1070 GOTO90

```

Note: For translation of the comments in German language pls. see preceding text.

Fig. 11.7.3

responsible for input of nominal value and of tolerance range. Instructions of lines 50 and 60 are for calculating the limit values G1 (minimum) and G2 (maximum) by considering nominal value and tolerance range. Lines 70 to 85 define functions which interpret the data, supplied to the ports, as BCD-coded information.

Function B(X) allocates the decimal digits 1000 and 100 to the 8 bits of port B. This is realized as follows: port B is read ($B = \text{PEEK}(40960)$) and the lower half byte is extracted by AND 240. The correcting value of $1/16$ is necessary for a correct decimal interpretation of the binary value. The digit position 1000 is realized by multiplication with 1000. Then the upper half byte is extracted by AND 15. In this case a correction is not necessary as the binary value corresponds to the decimal one. The digit position 100 is realized by multiplication with 100. This value is added to the thousands. By a similar way tens and units are generated.

However, the procedure for getting the tenthousand digit position differs from the forementioned one. In this case the TTY-KYBD-line is utilized. It can be scanned by Z32 at PB6, whereby all other lines of port B are extracted from Z32 by AND 64. The correcting value refers to the binary digit position G4. This value is determined as highest decimal position by multiplication with 10000.

Now the initializing has been finished.

Lines 90 to 210 are for the following functions:

- 90: Key scanning. If "M"-key was pushed, then go to subroutine "ZWISCHEN-WERTE" (=intermediate values).
- 100: If flag is set, then read measured value.
- 110: If not, then return to key scanning.
- 120: Read values of ports.
- 130: Calculate decimal value, increment counter for the number of measured values, generate average.
- 140: If the measured value is lower than the tolerance minimum, then jump to "AUSGABE AM LINKEN RAND" (=output at left side).
- 150: If the measured value is lower than the tolerance maximum, then jump to "AUSGABE IN DER MITTE" (=output in the middle).
- 160: Output of measured value at the right side.
- 170: Return to key scanning.
- 180: Output for the left side, increment counter for too low values.
- 190: Return to key scanning.
- 200: Output for the middle, increment counter for the correct value.
- 210: Return to key scanning.

Line 1000 is reached by operating the M-key. The instructions following to line 1000 are for printing the total number of measured values, the average and the assignment to the tolerance range.